A Compiled 3.5fJ/conv.step 9b 20MS/s SAR ADC for Wireless Applications in 28nm FDSOI

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Norwegian University of Science and Technology
Nordic Semiconductor

Key contribution 1

Q. Can a DRC/LVS clean SAR ADC be compiled from text files, and have state-of-the-art performance?

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Netlist
(SPICE)

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Object definition
(JSON)

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Netlist
(SPICE)

Object definition
(JSON)

Technology rules
(JSON)

Key contribution 1

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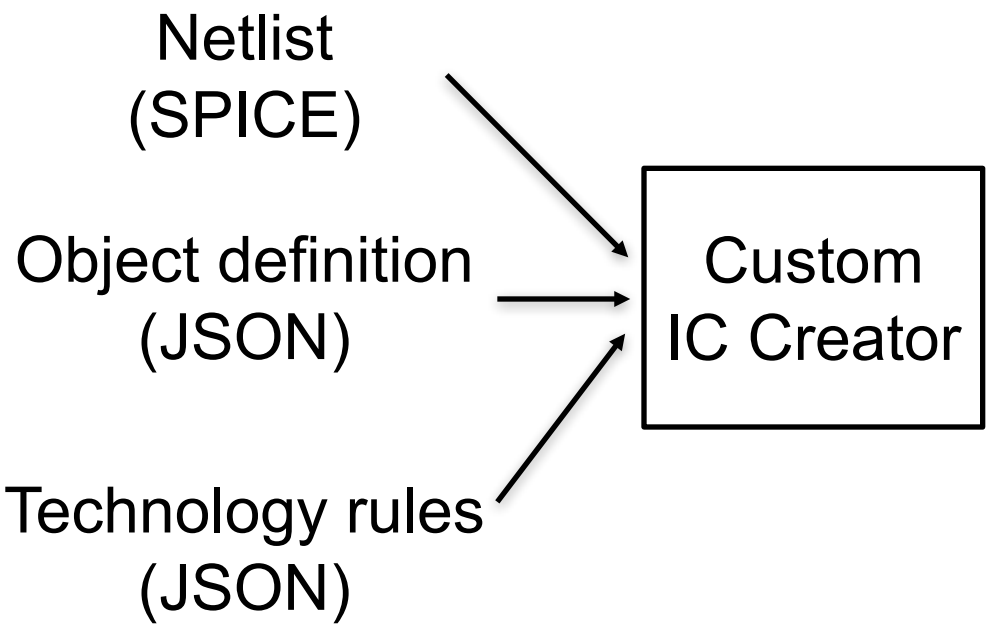

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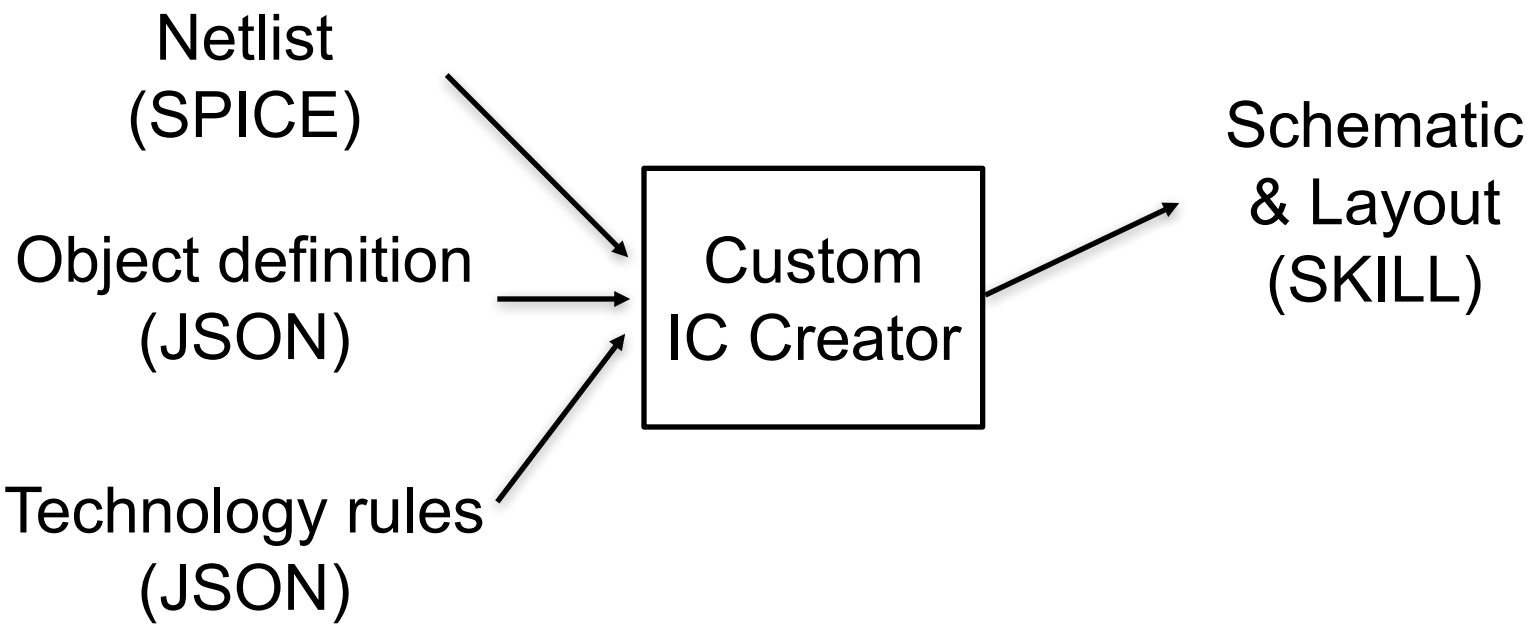

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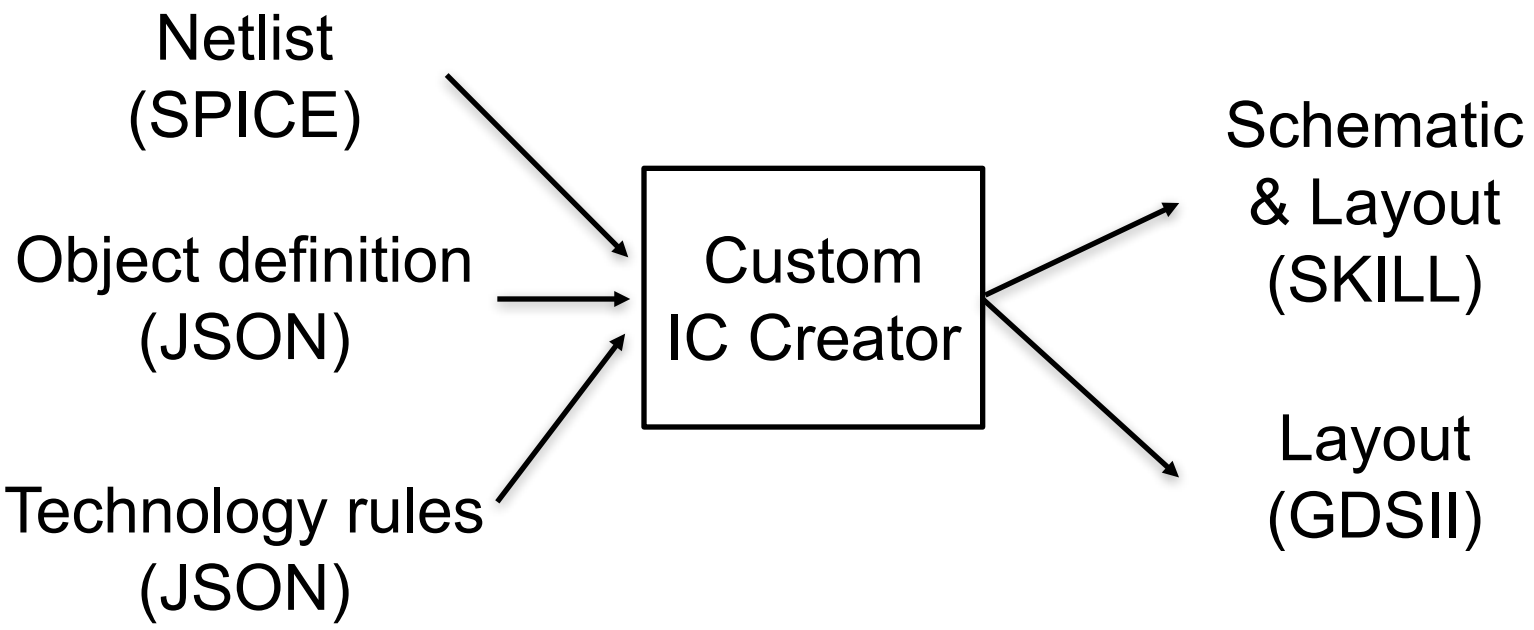


Netlist

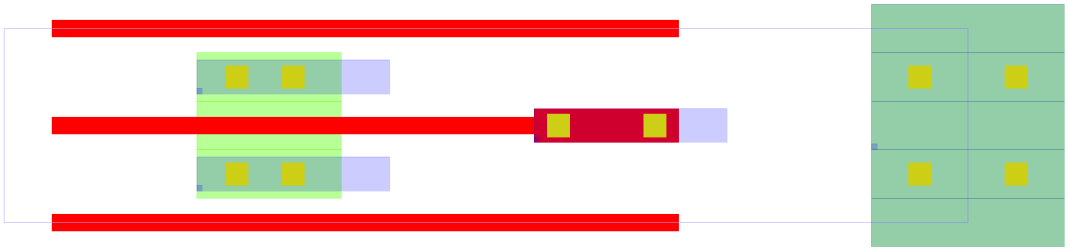
```
.SUBCKT IVX1_CV A Y AVDD AVSS
    MN0 Y A AVSS AVSS NCHDL
    MP0 Y A AVDD AVSS PCHDL
.ENDS IVX1_CV
```

Row 0, Colum 0

Row 0, Colum 1

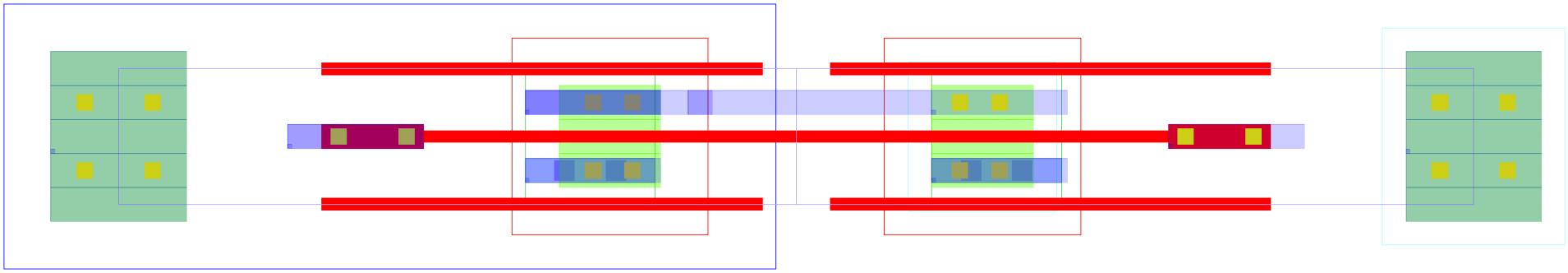
Object definition file - Unit transistor

```
{ "name" : "DMOS" ,
  "class" : "Gds::GdsPatternTransistor"
  "fillCoordinatesFromStrings" : [
    [   "OD",
    "------------------xxxx",
    "----xxK-----------xCxC",
    "----xxx-----------xxxx",
    "----xxK-----------xCxC",
    "------------------xxxx"],
    [   "PO",
    "-mmmmmmmmmmmmm--------",
    "----------------------",
    "-mmmmmmmmmmcxc--------",
    "----------------------",
    "-mmmmmmmmmmmmm--------"],
    [   "M1",
    "------------------xxxx",
    "----wDww----------xxxx",
    "-----------wGww---xBxx",
    "----wSww----------xxxx",
    "------------------xxxx"]
]}
```

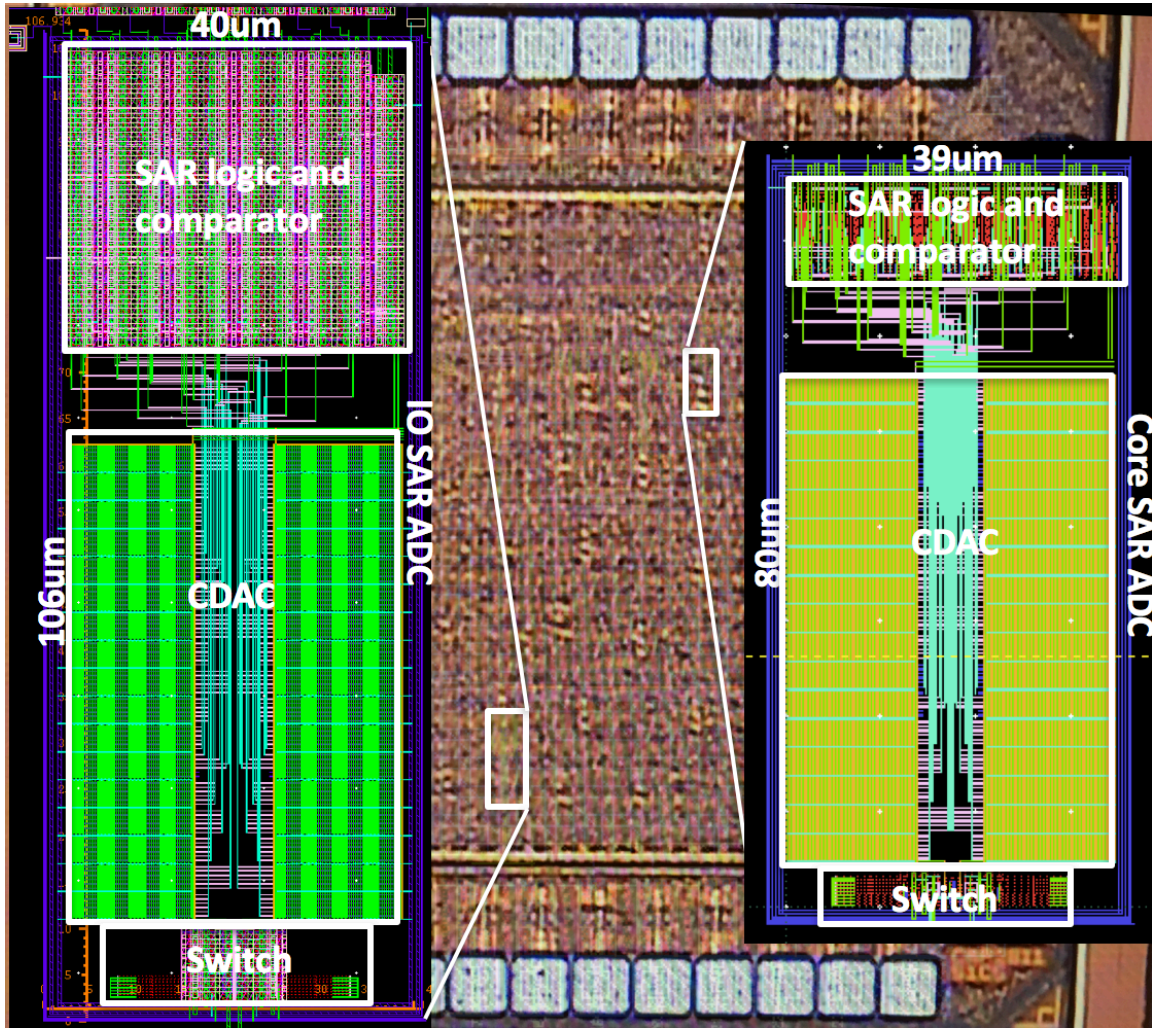


Object definition file - Inverter

```
{ "name": "IVX1_CV" ,
    "class" : "Layout::LayoutDigitalCell"
    "beforeRoute" : {
      "addDirectedRoutes" : [
         ["M1","Y","MN:D-|--MP:D"],
         ["PO","A","MN:G-MP:G"]
    ]
  }
}
```



Complete SAR ADCs



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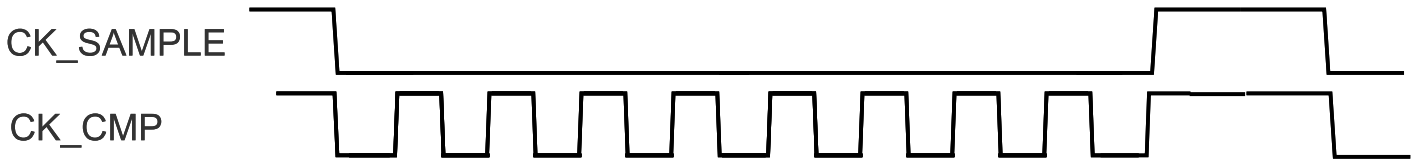

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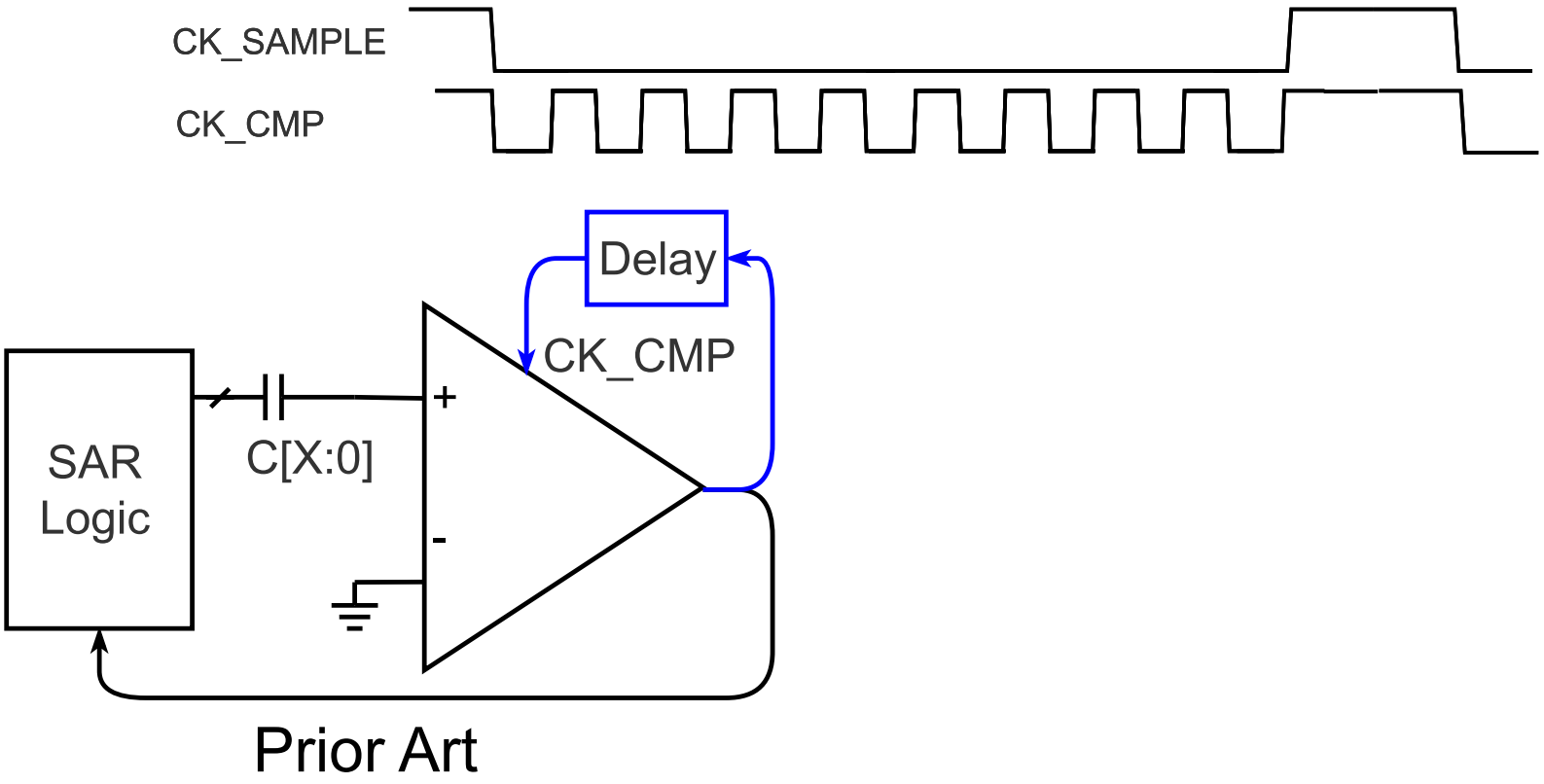

Prior Art

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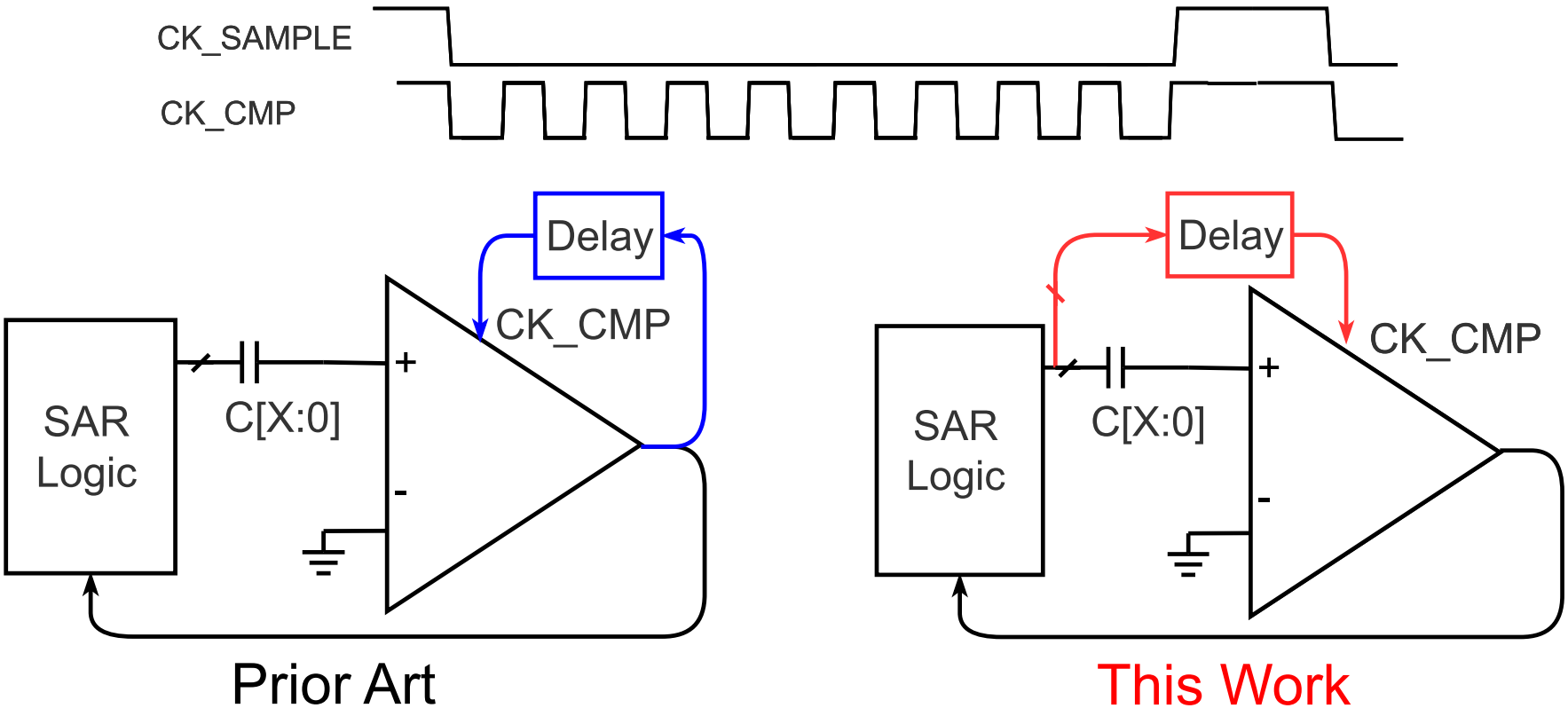
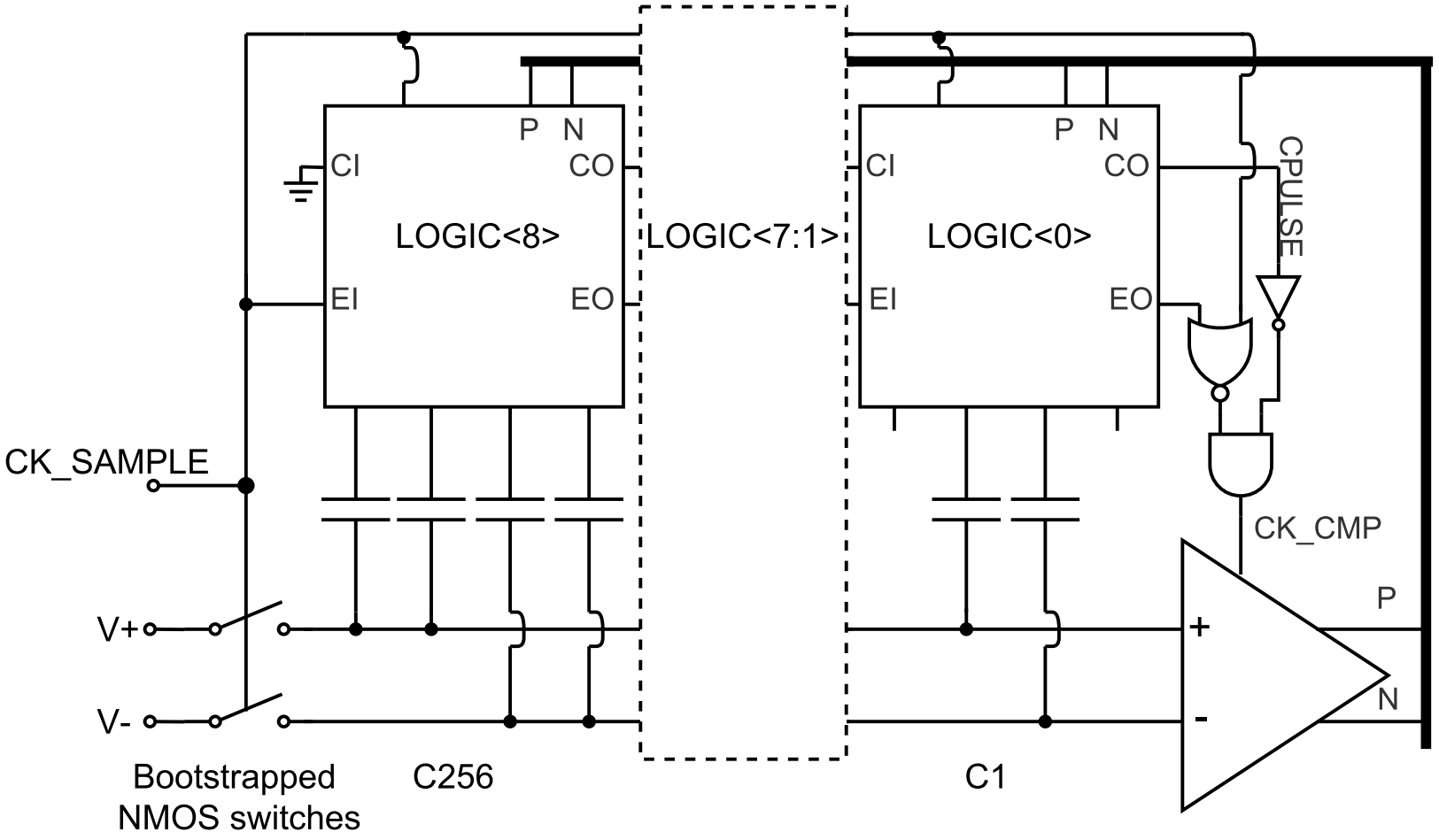


SAR ADC Architecture



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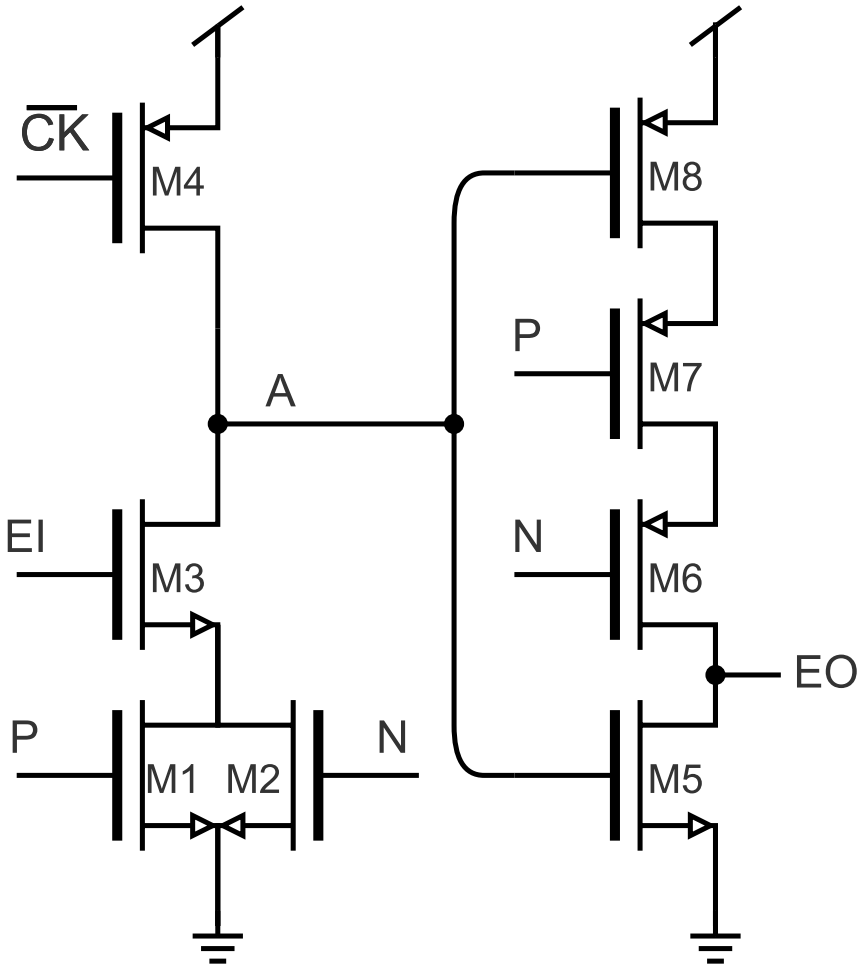
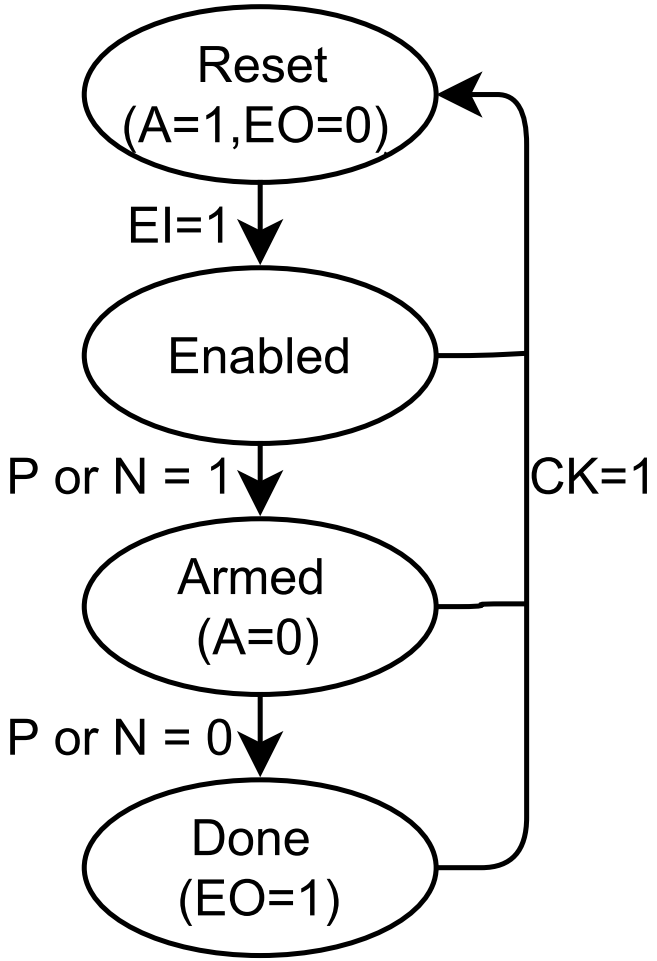
Enable logic





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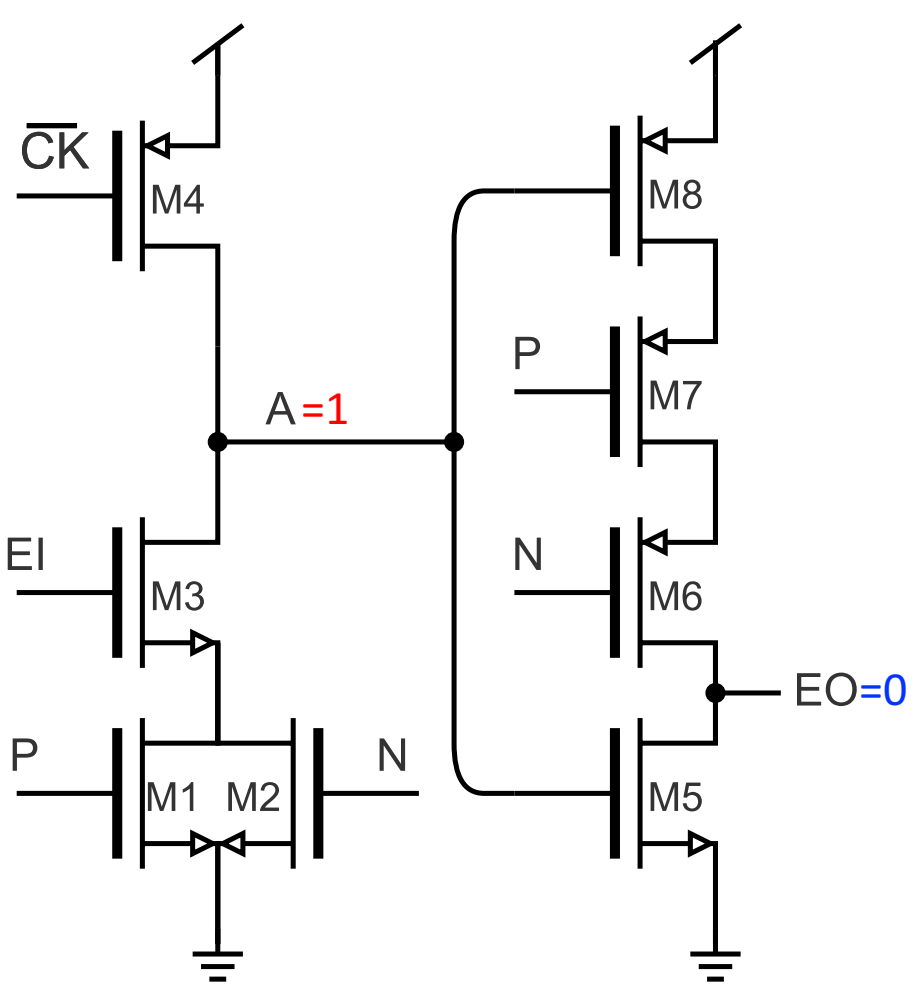

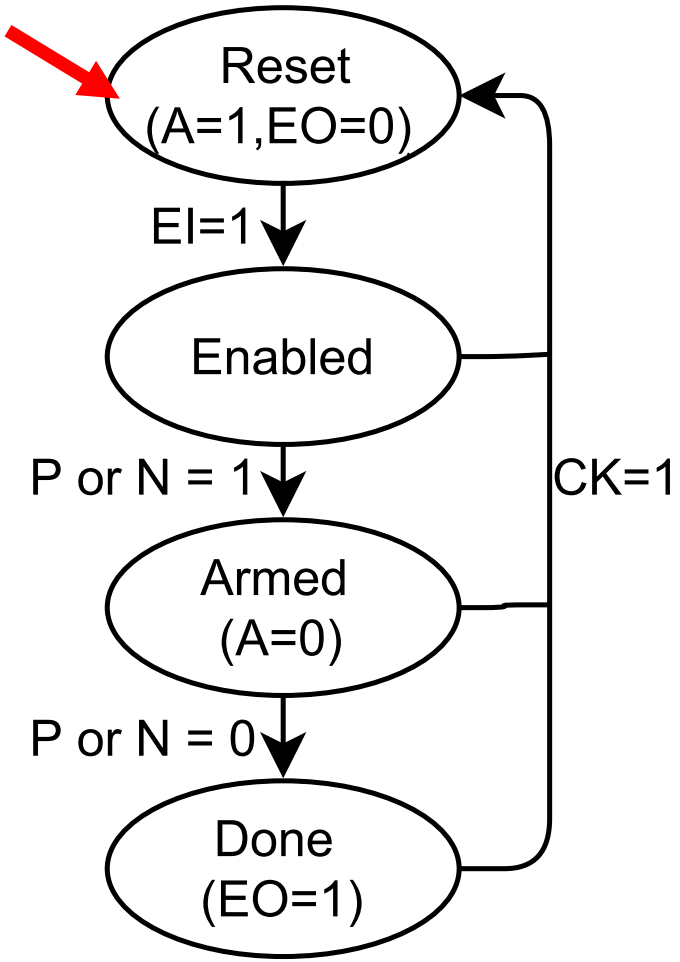

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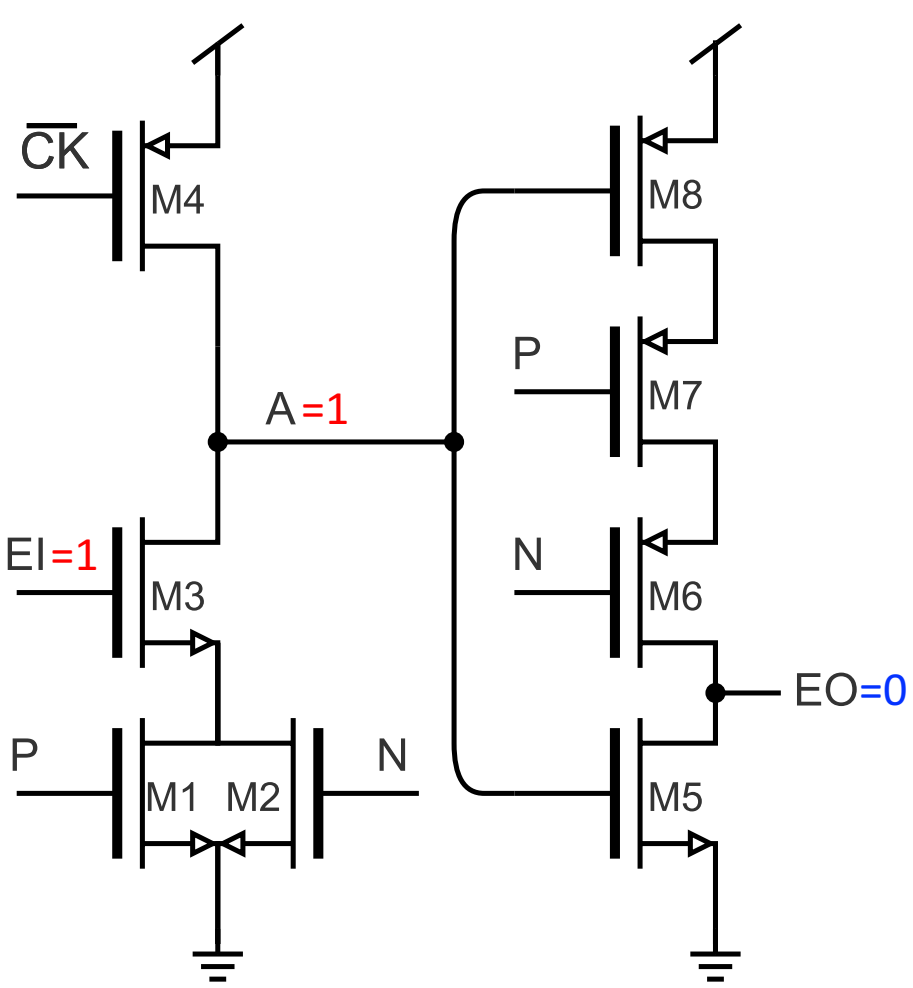

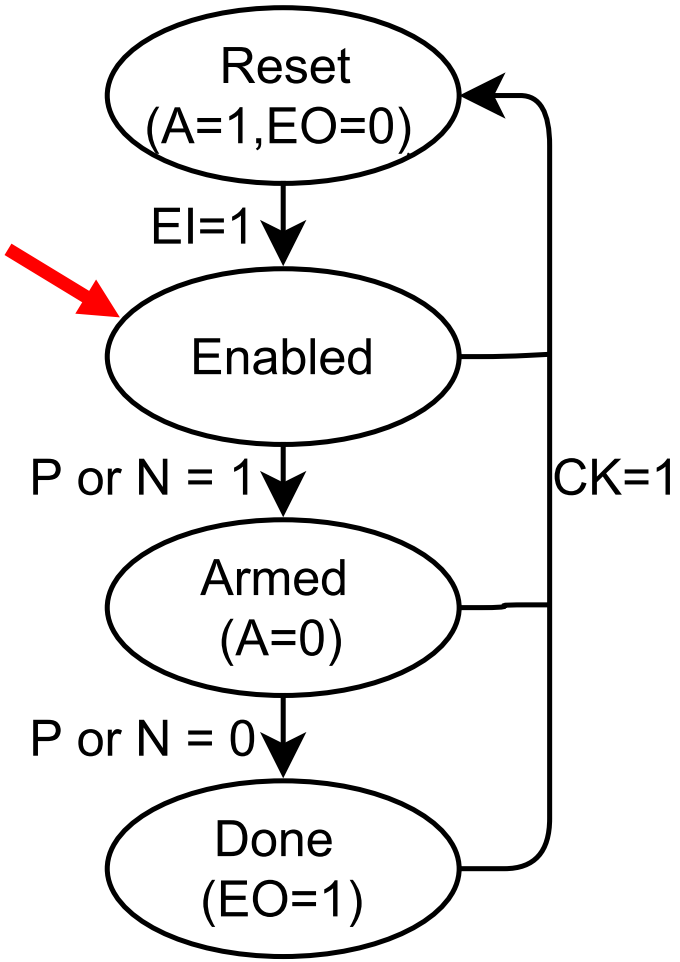

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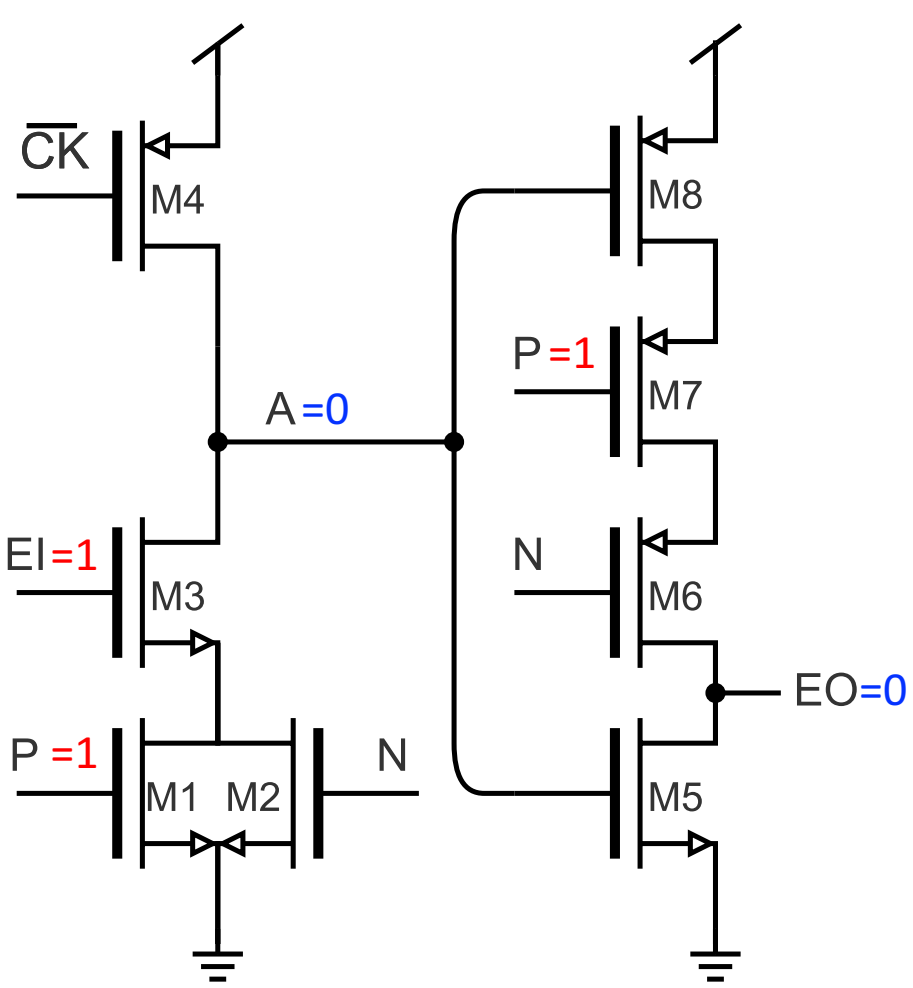

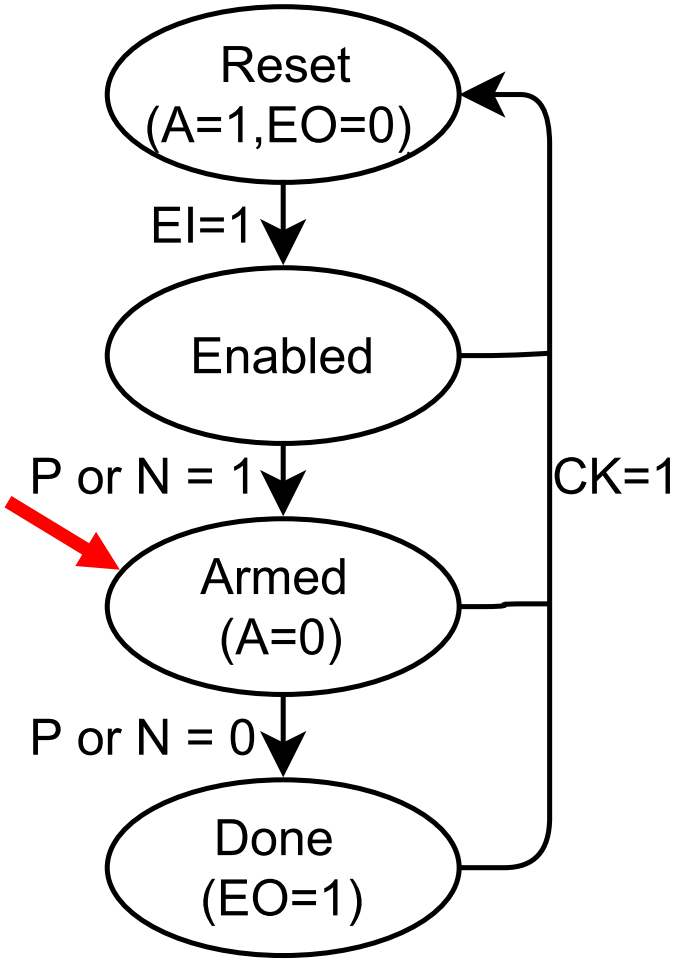

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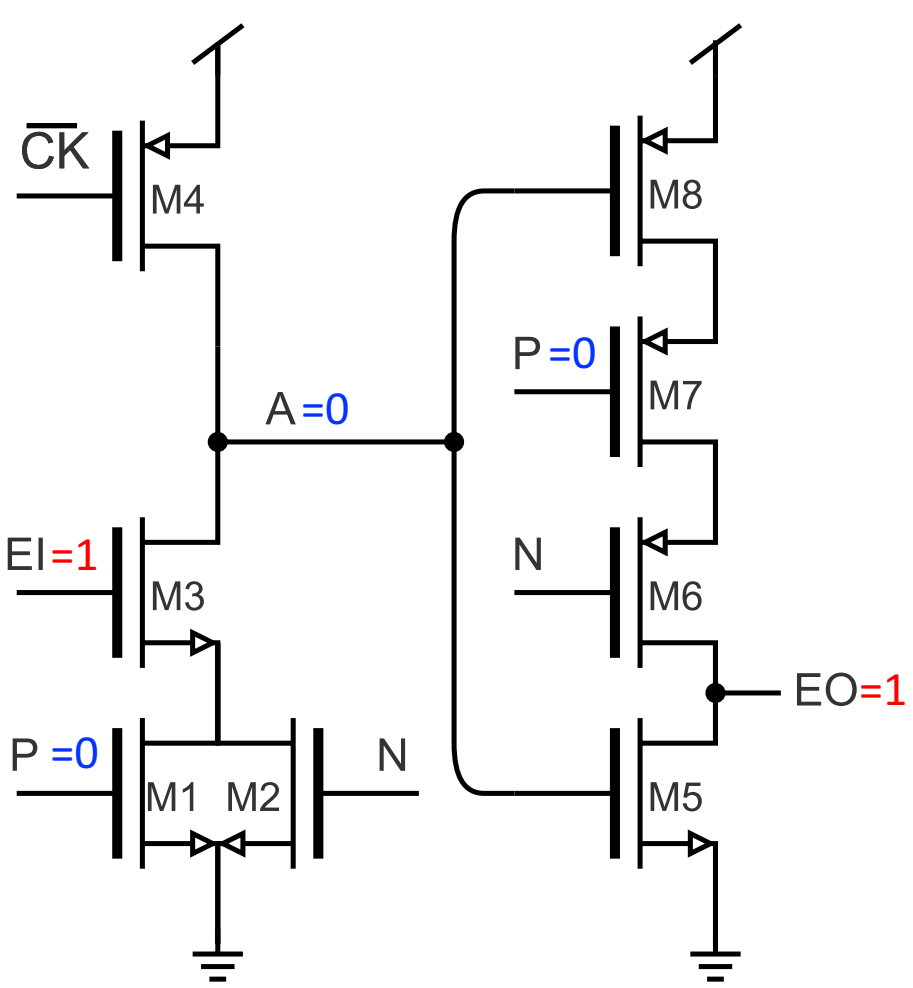
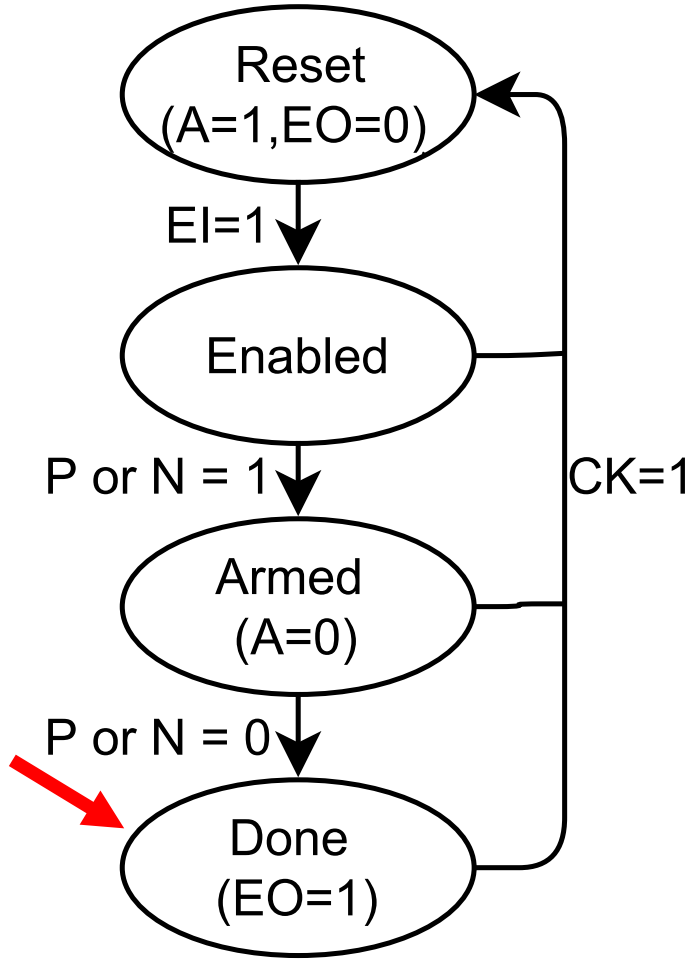
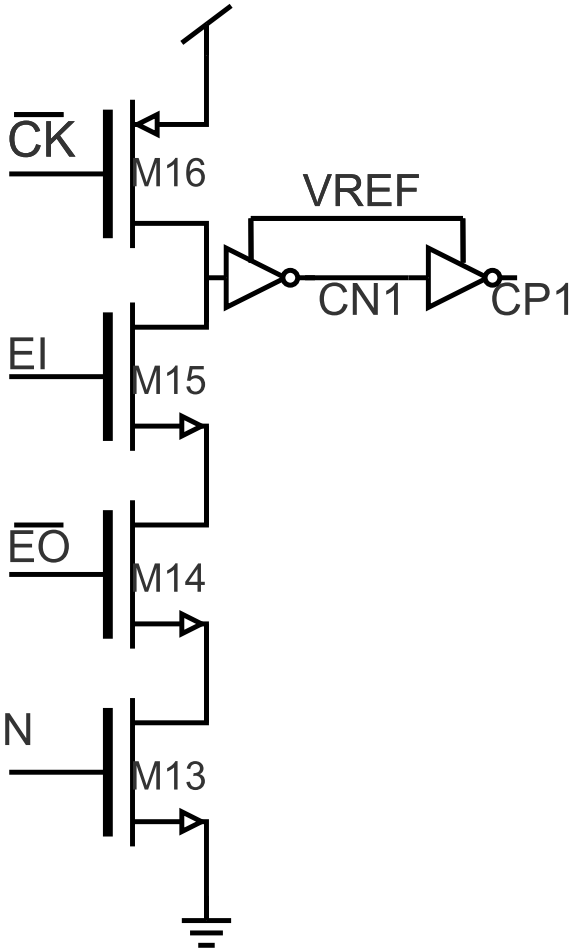
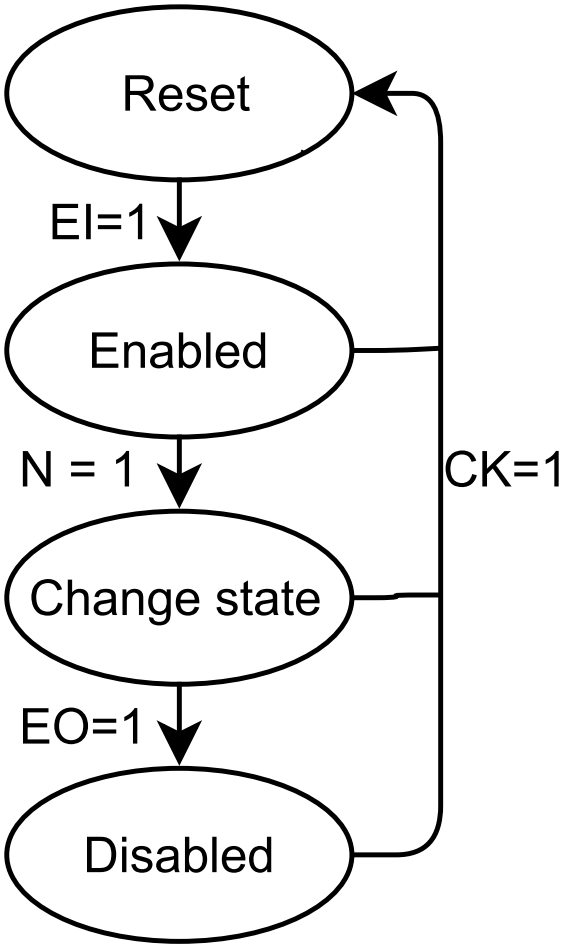




CDAC Statecontrol





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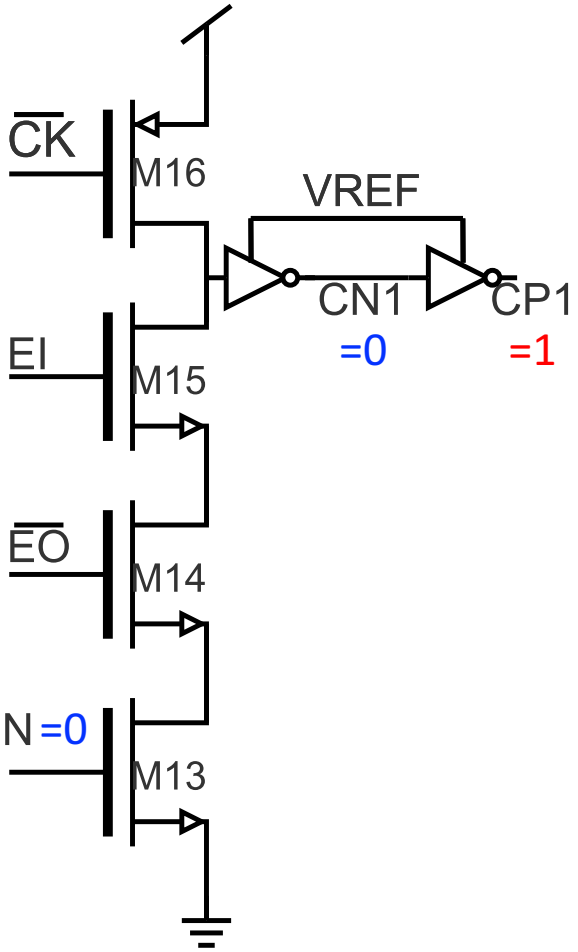

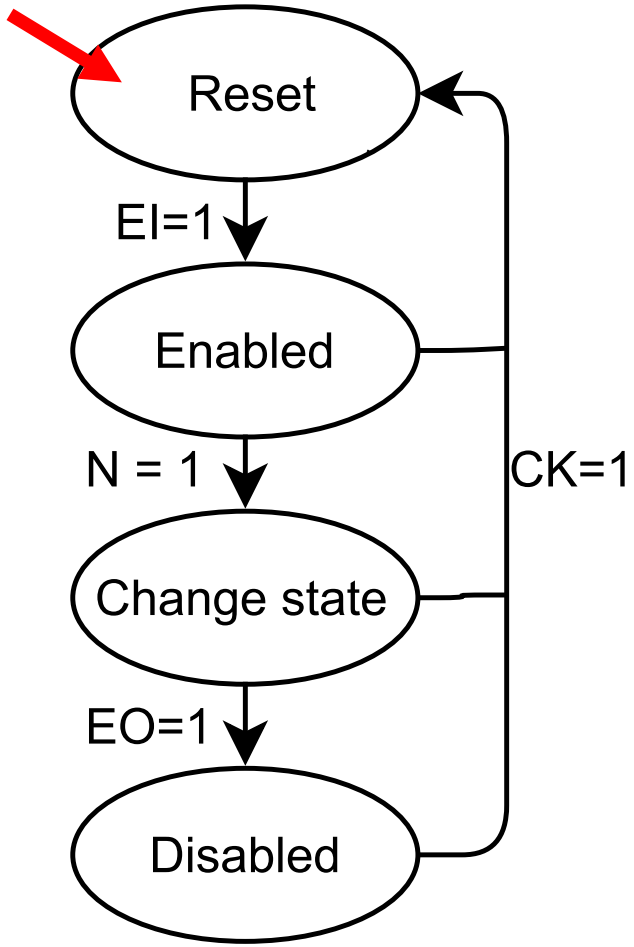

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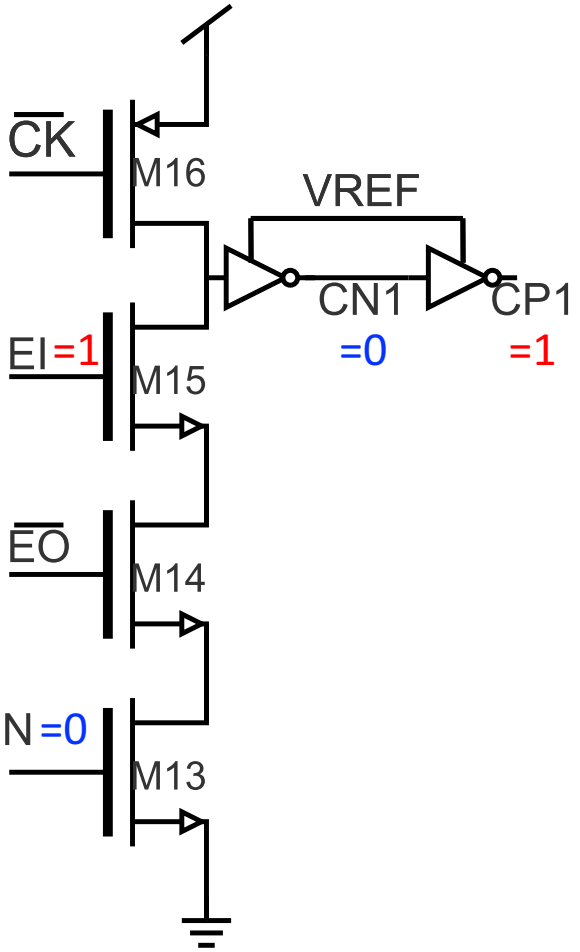

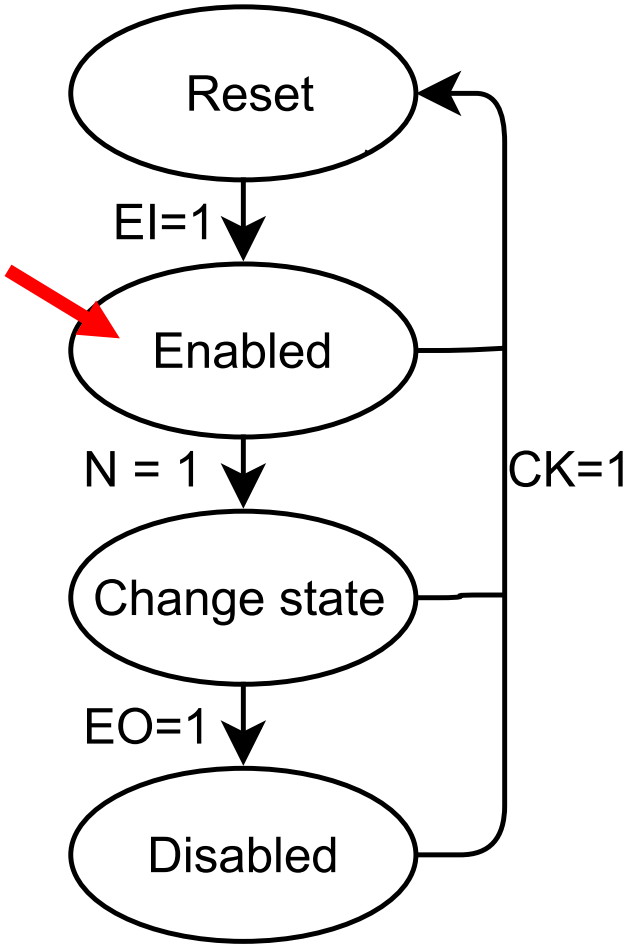

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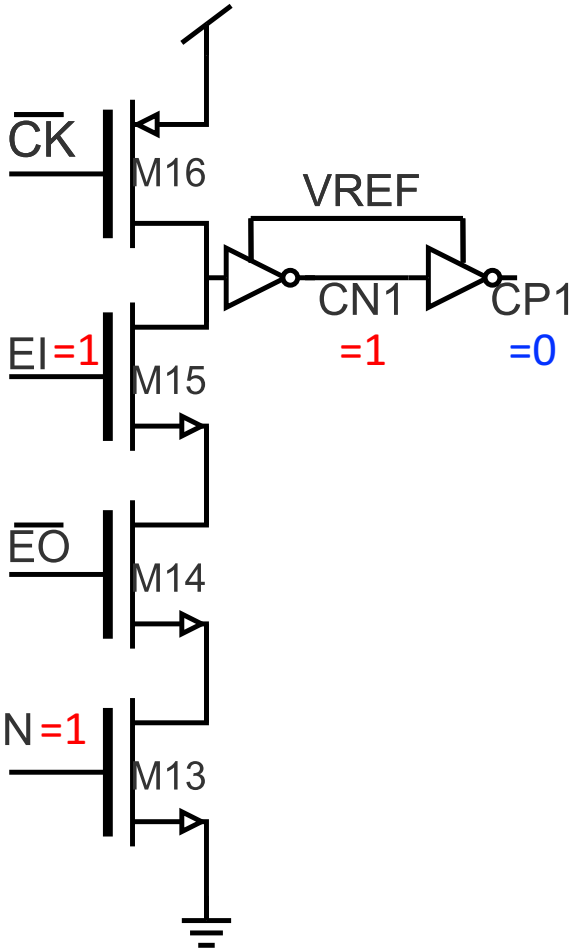

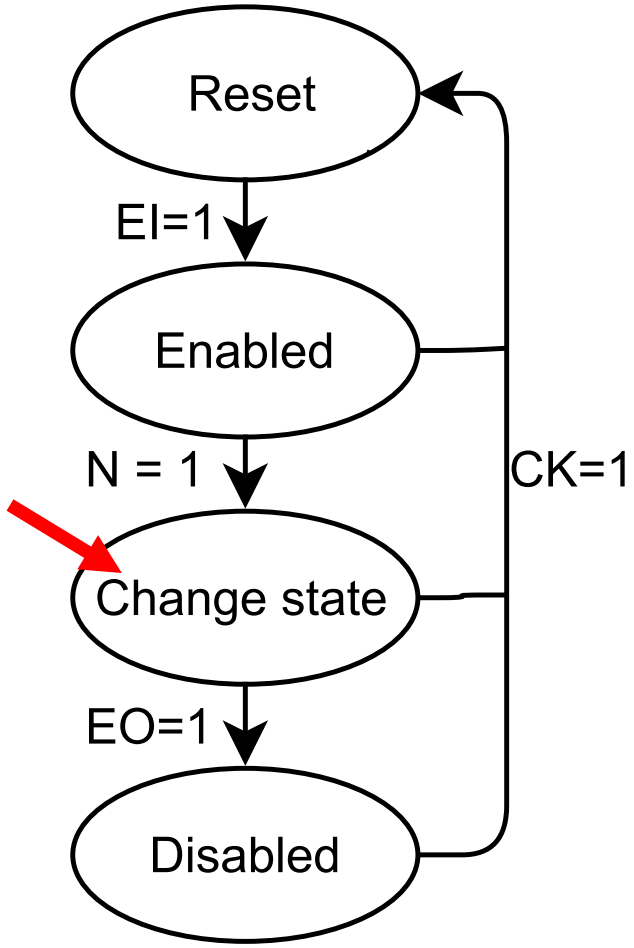

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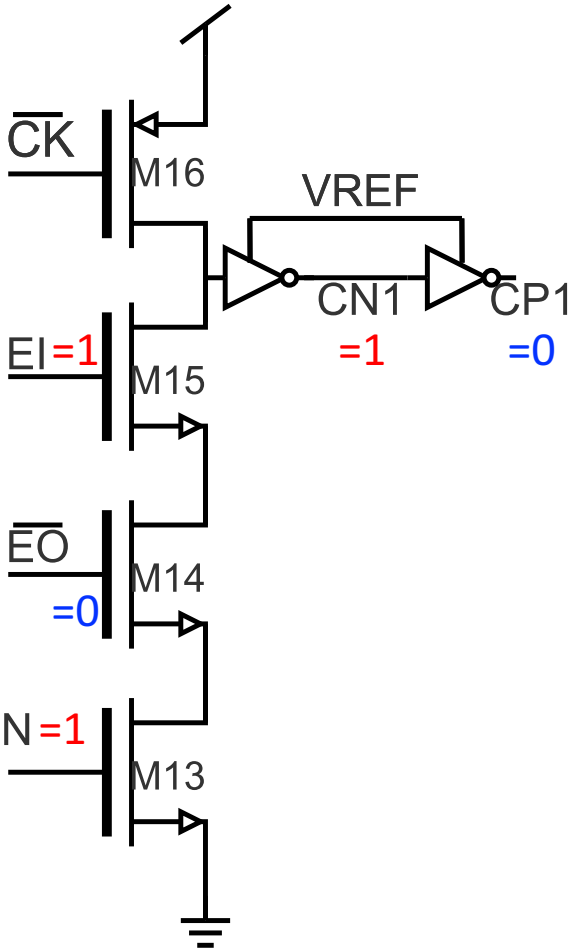
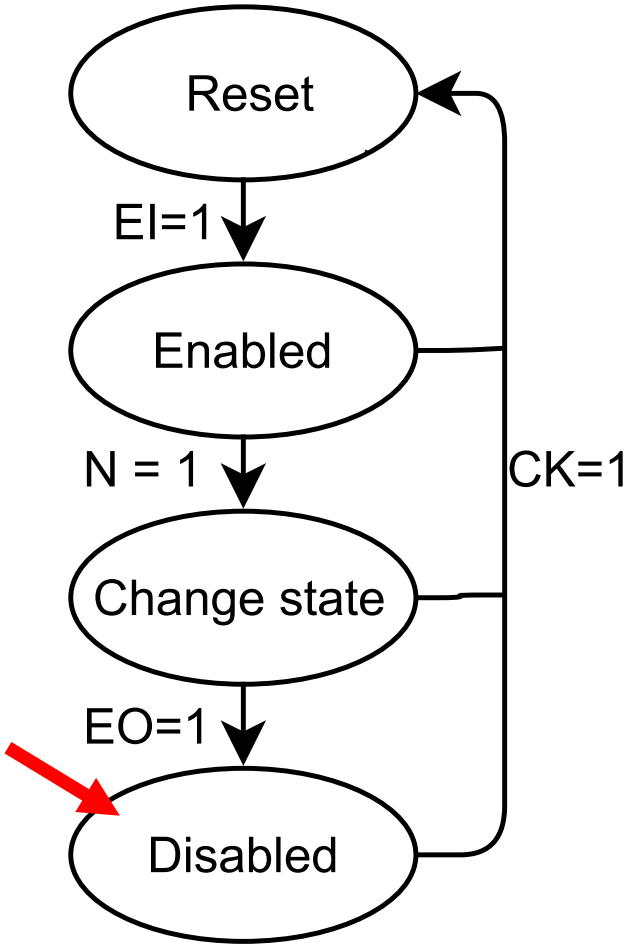
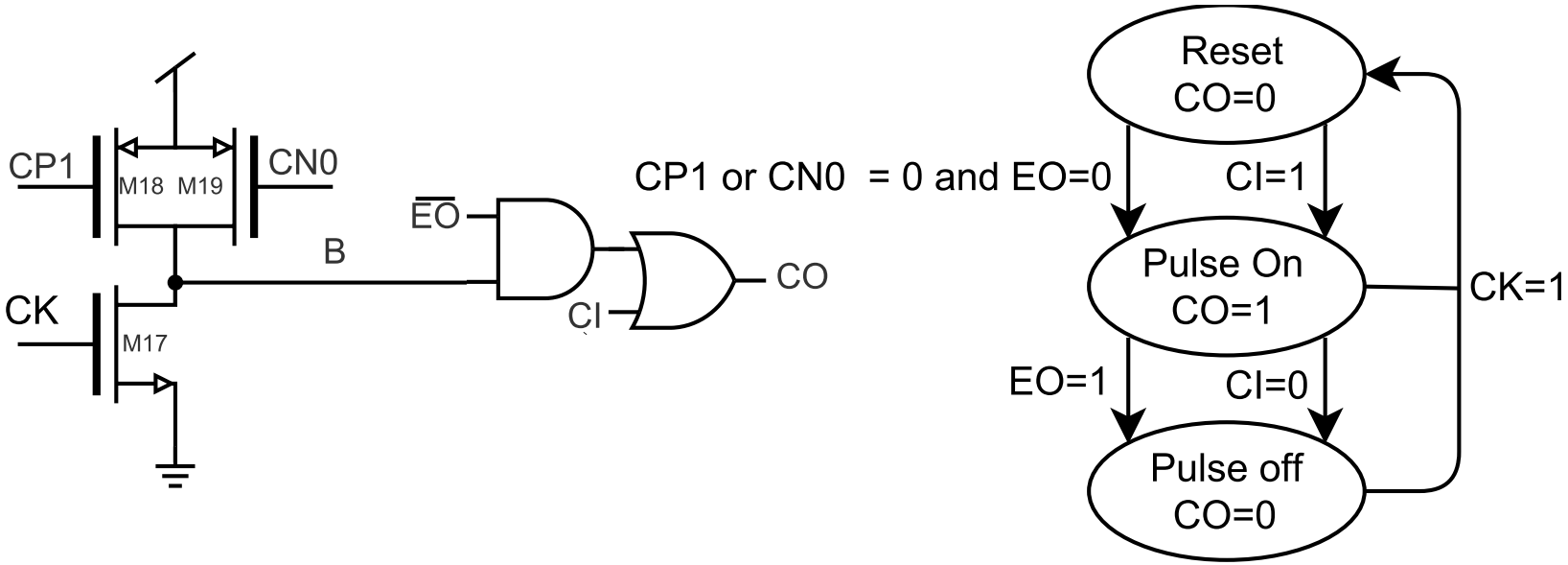


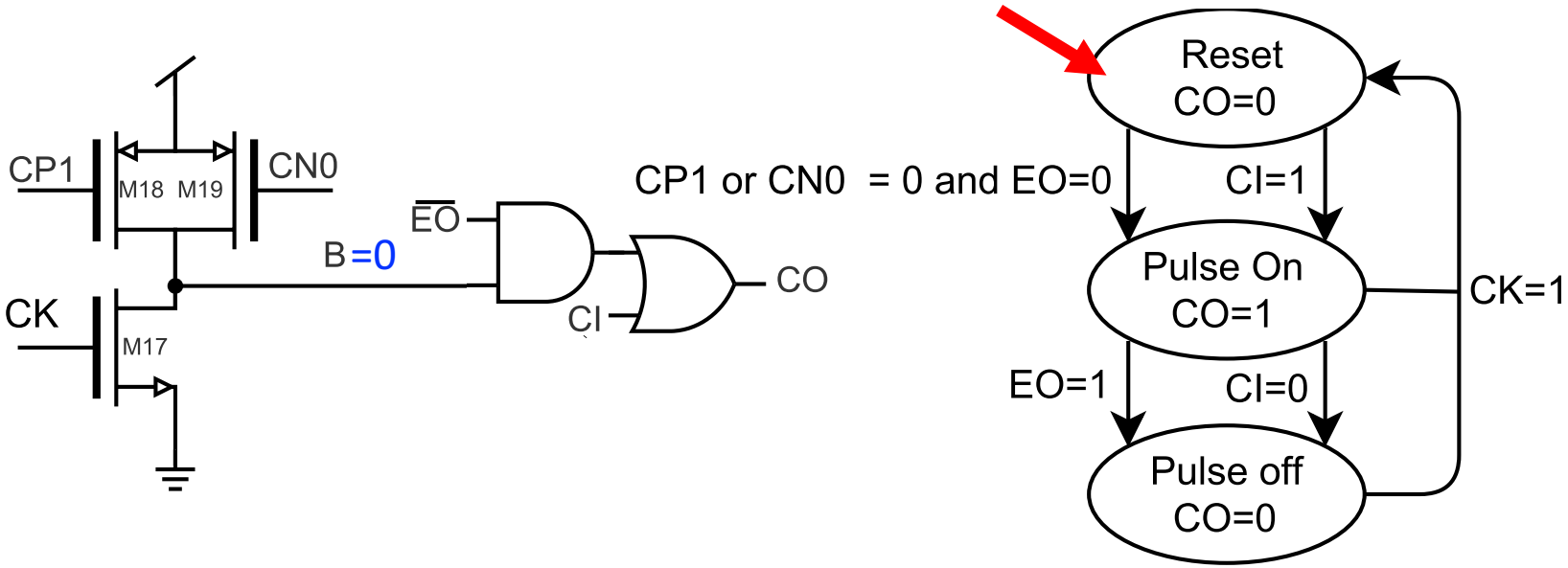


Clock generation



Key contribution

Clock generation



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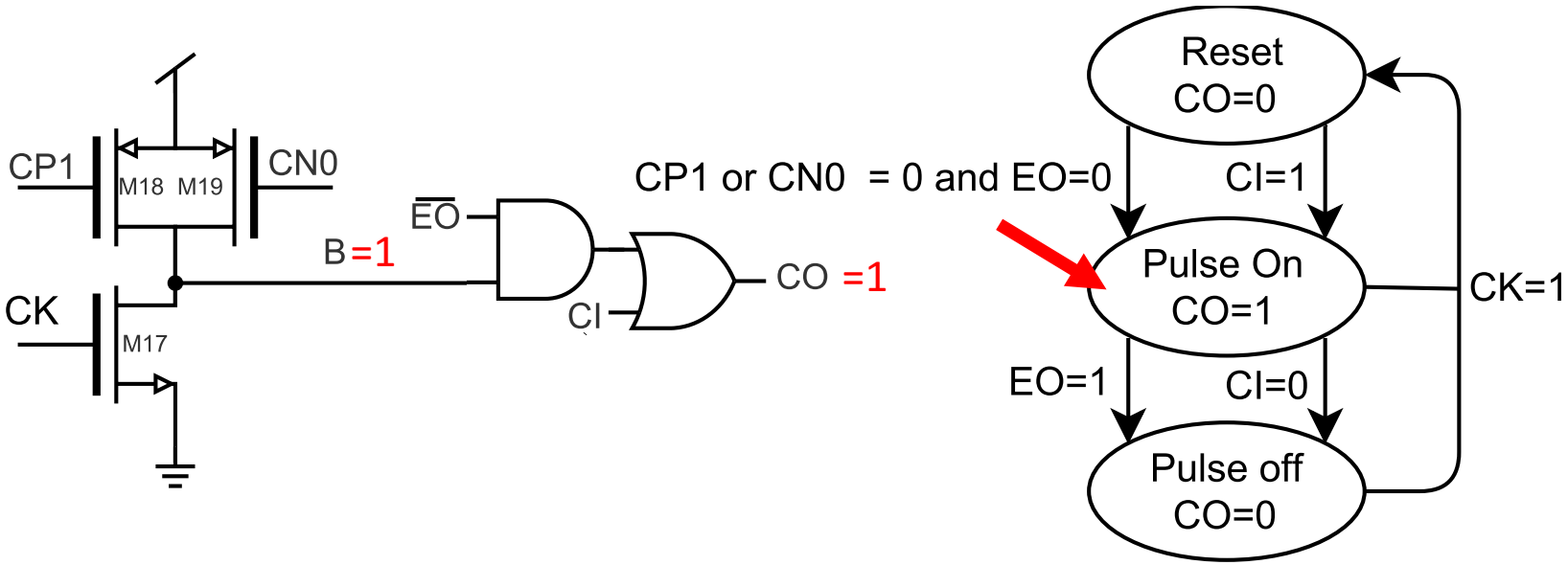

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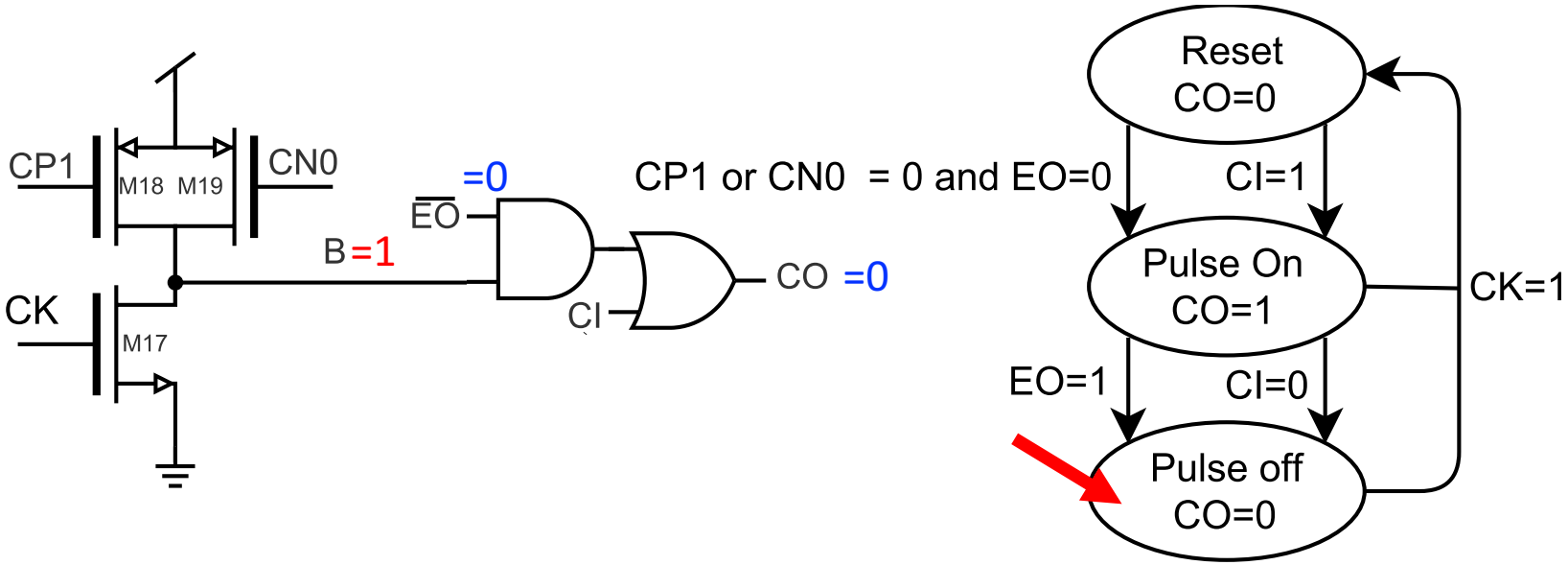
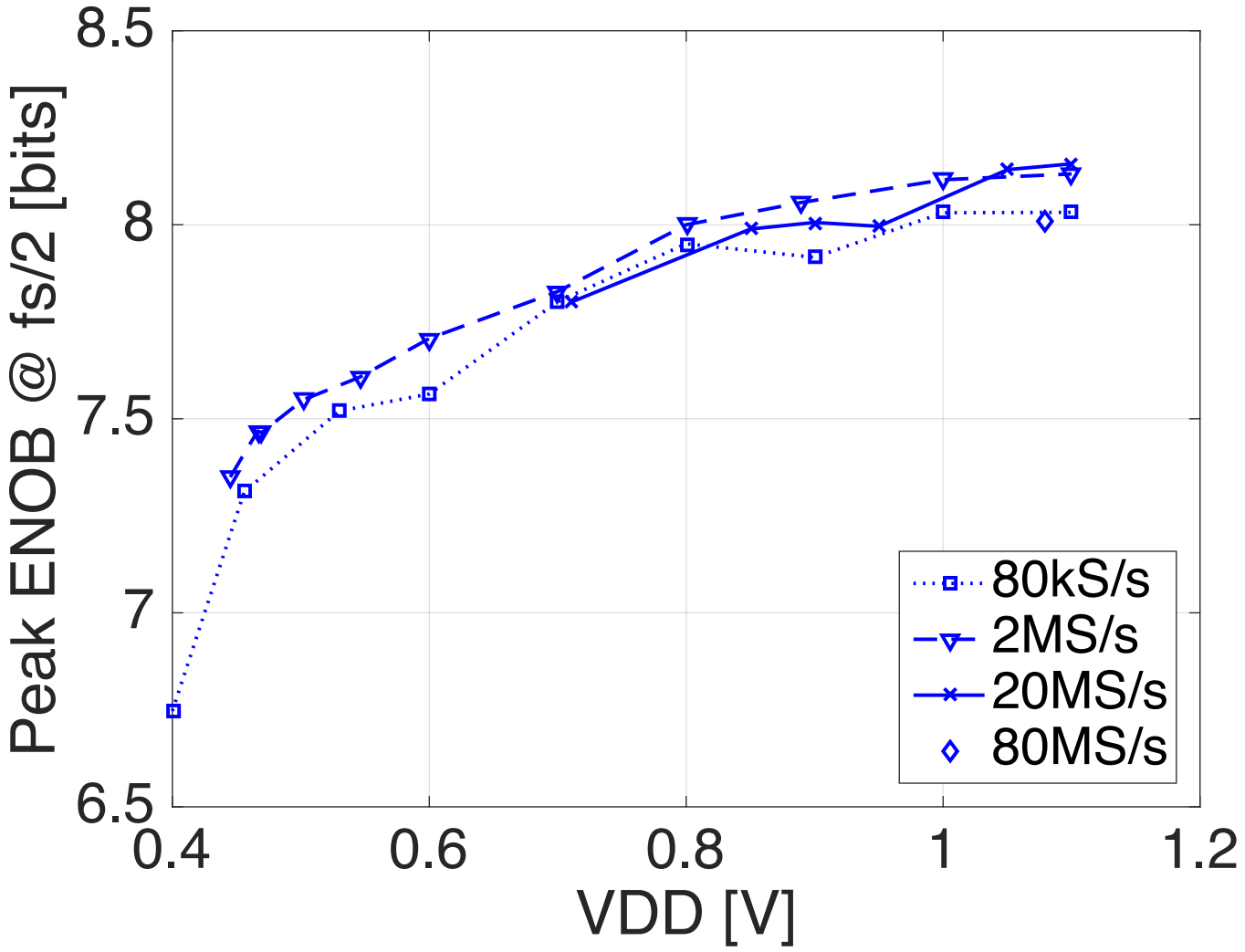
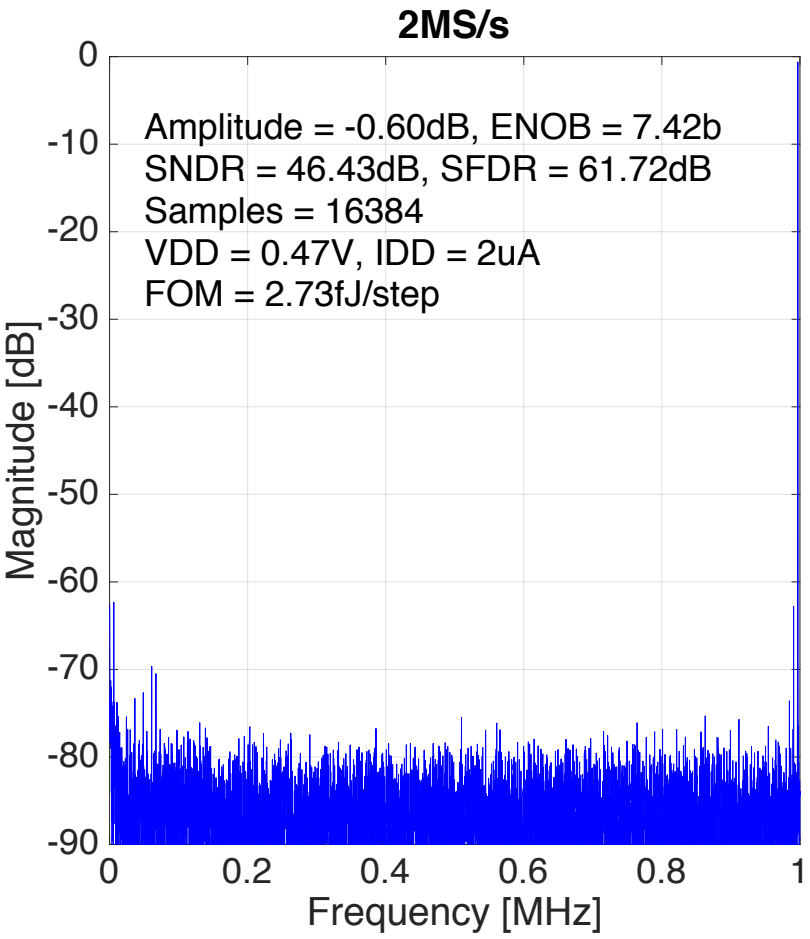


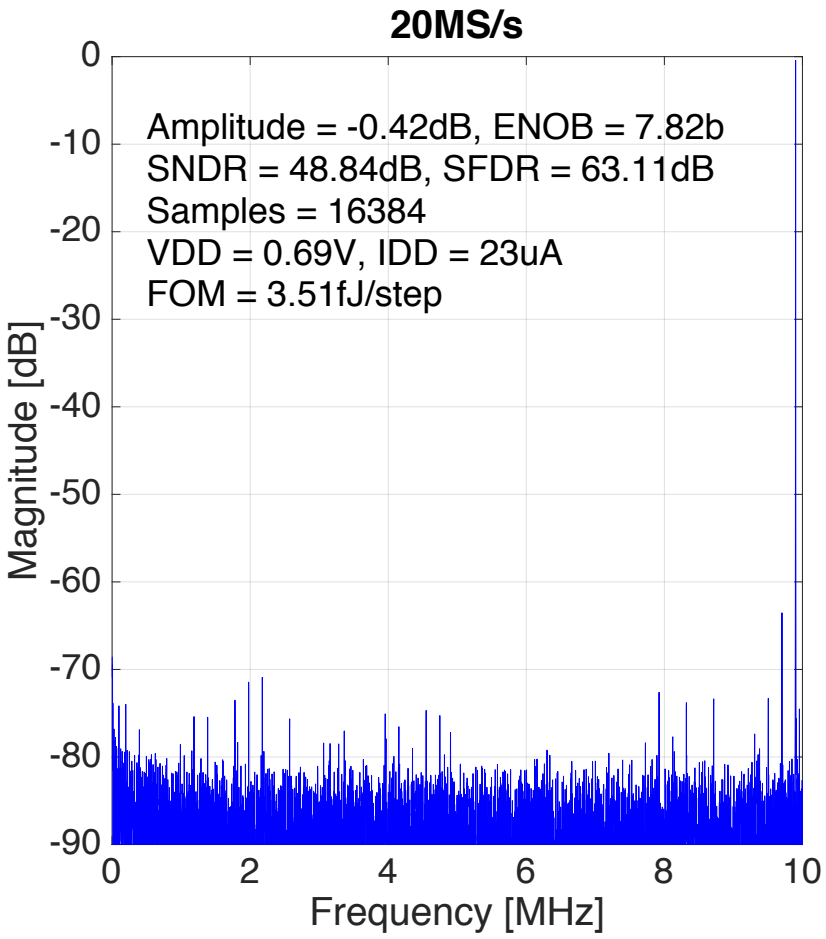
Key contribution

Peak ENOB as a function of VDD

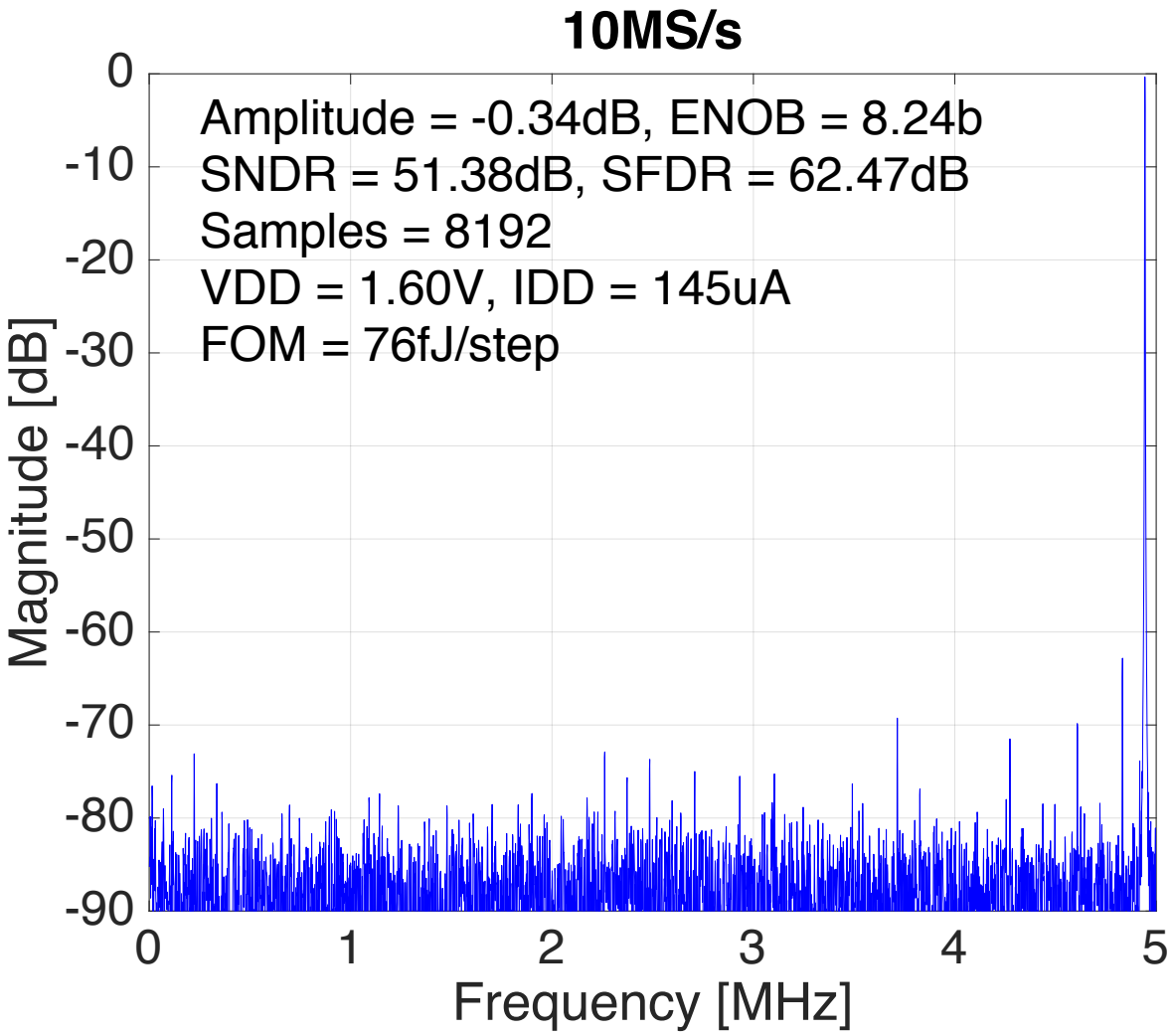


Core transistor SAR ADC





IO transistor SAR ADC

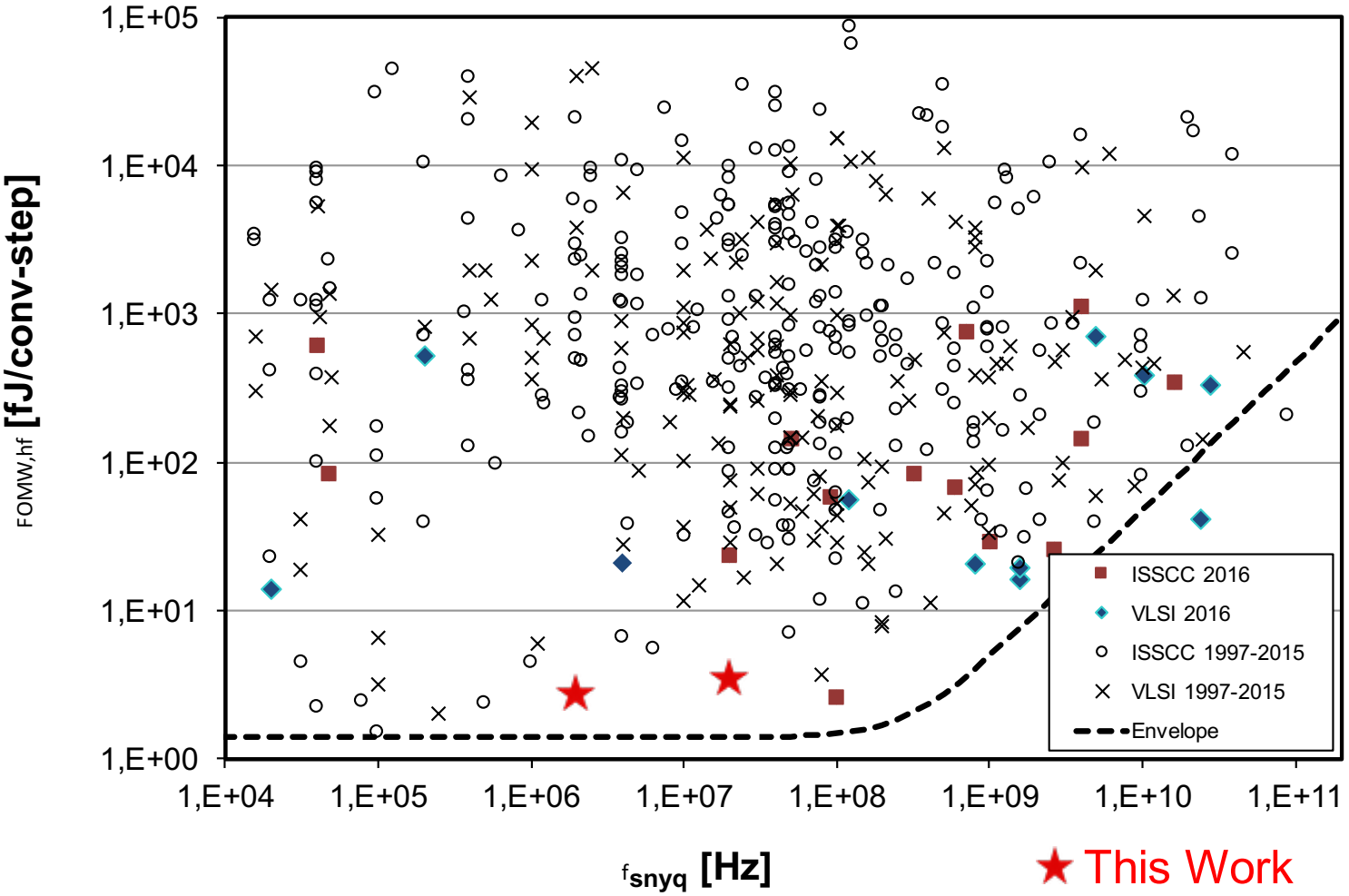


Comparison to prior art

	[A]	[B]	This work		
Technology [nm]	90	90	28 CORE		28 IO
Fsample [MS/s]	21	2	2	20	10
Core area [mm^2]	0.18	0.047	0.0032		0.0042
ENOB [bits]	5.45	6.7 - 9.4	7.42	7.82	8.24
SFDR [dB]	40.81	72.33	61.72	63.11	62.47
Power [µW]	1110	1.6 – 3.6	0.94	15.87	< 145
Supply [V]	0.7	0.7	0.47	0.69	1.6
FOM [fJ/c.step]	838	2.8 – 6.6	2.74	3.51	< 76

[A] S. Weaver, B. Hershberg, and U. K. Moon, “Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells,” *IEEE Trans- actions on Circuits and Systems I: Regular Papers*, vol. 61, no. 1, pp. 84–91, Jan 2014.
[B] P. Harpe, G. Dolmans, K. Philips, and H. de Groot, “A 0.7V 7-to-10bit 0- to-2MS/s flexible SAR ADC for ultra low-power wireless sensor nodes,” in *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, Sept 2012, pp. 373– 376.

Comparison to state-of-the-art



B. Murmann, "ADC Performance Survey 1997-2016," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

Conclusion

A DRC/LVS clean SAR ADC can be compiled from text files, and have state-of-the-art performance.

C++ version of compiler*

Thank you for your attention!

https://github.com/wulffern/ciccreator

https://github.com/wulffern/ciccreator/blob/master/examples/SAR_ESSCIRC16_28N.json
https://github.com/wulffern/ciccreator/blob/master/examples/SAR_ESSCIRC16_28N.spi

* Does not have all the features of Perl compiler, and can't do full SARs. Yet.