Resonators in Open-Loop Sigma-Delta Modulators

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***Abstract*—In this paper we introduce the modulo resonator for use in *open-loop sigma-delta modulators* (OLSDM). The OLSDM presented in this work is intended for use in high accuracy (14-bit), high-speed analog-to-digital converters.**

The modulo resonator is used with a modulo notch filter to insert a zero in the noise transfer function at a non-zero frequency. The effect of finite gain in modulo integrators and modulo resonators are described and verified through simulation. The modulo resonator and previously published modulo integrator are used in a behavioral model of a switched-capacitor fifth-order OLSDM with more than 13-bit effective number of bits for an oversampling ratio of four. We prove for the N-order OLSDM that the number of bits in the quantizer (B) must be larger than N to ensure equivalence between OLSDM and sigma-delta modulation.

***Index Terms*—Sigma-delta modulators, switched-capacitor circuits, modulo integrator, modulo resonator, open-loop sigma-delta modulators**

I. Introduction

Open-loop sigma-delta modulators are a sub group of sigma-delta modulators. We define OLSDM as *any sigma-delta modulator that does not have feedback of the quantized modulator output signal*.

An example of analog-to-digital conversion with OLSDM is shown in Fig. 1. The input signal, x, is accumulated by the integrator ($\langle\Sigma\rangle$). The integrator in Fig. 1 is a modulo integrator that wraps around when the sum exceeds the range (R). The output of the integrator (u) is quantized by a quantizer, which is modeled as a linear addition of quantization noise (q). The conditions for modeling a quantizer as linear addition of noise was covered in [1]. The modulo differentiator ($\langle\Delta\rangle$) reverse the effect of the modulo integrator. The decimation filter required to down-sample the output of the modulator is not shown.

In this modulator the input signal passes through unchanged. The quantization noise pass through the differentiator and is first order high-pass filtered.

The sigma-delta modulator in Fig. 1 is equivalent to a first order low-pass sigma-delta modulator providing certain conditions are met.

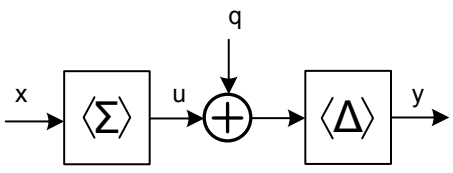

Fig. 1. First order low-pass open-loop sigma-delta modulator

One of the first suggestion of an OLSDM was in [2]. Although there was no system implementation they explained a method that avoided feedback of the quantized signal. More recently there have been others like the Frequency Sigma-Delta Modulator (FSDM) in [3] and [4]. In the FSDM a voltage controlled oscillator (VCO) is used as the modulo integrator, and it was shown in [3] that the pre-processing in FSDM is equivalent to modulo integration. The non-feedback sigma-delta digital-to-analog modulator, where the integrator is implemented as a digital modulo integrator, was described in [5]. In [6] an amplitude modulated switched-capacitor open-loop sigma-delta modulator was introduced. A switched-capacitor modulo integrator was used to perform the modulo integration.

The application envisioned for OLSDM is as a front-end in a high speed (>10MS/s), high resolution (14-bit) analog-to-digital converter. The advantage of OLSDM is that it is trivial to use high-latency quantizers since there is no feedback of the quantized modulator output.

There are two unsolved challenges that this paper discuss: when is open-loop sigma delta modulation equivalent to sigma-delta modulation, and how to introduce zeros in the noise transfer function (NTF) at non-zero frequencies.

A. When is OLSDM equivalent to SDM?

It is observed in simulation that open-loop sigma-delta modulation (OLSDM) is not always equal to sigma-delta modulation (SDM). Whether an OLSDM works as an SDM depends on the input signal amplitude and the number of bits in the quantizer. The input signal amplitude must be less than $|x_n| < R/2$ (0dBFS[1]), but OLSDM sometimes loose its noise shaping at less than 0dBFS.

In [6] an error correction scheme was used to restore the noise shaping for input signal amplitudes up to 0dBFS. But the error correction assumed that the input frequency was much less than the sampling frequency ($f_i << f_s$). For some applications (like high speed, high resolution) the OSR can be low ($OSR < 8$) and $f_i << f_s$ is no longer valid.

The number of bits in the quantizer affect the equivalence between OLSDM and SDM. It is observed that the number of bits in the quantizer must be larger than the order of the modulator. This was proved for the special case of a second order OLSDM in [7].

We will prove for the N-order OLSDM that the number of bits in the quantizer (B) must be larger than the order (N) to ensure equivalence between OLSDM and SDM.

B. Zeros in NTF at non-zero frequency

Previous OLSDMs have all been low order low-pass sigma-delta modulators. Low order low-pass sigma-delta modulators

[1]0-dB referred to full scale amplitude, $R/2$

are unsuited for high conversion rate applications due to the high oversampling ratio required to get high resolution, assuming a low resolution quantizer is used.

If the sampling frequency (f_s) is constant, the resolution can be increased by adding more zeros to the noise transfer function (NTF). Adding zeros at a non-zero frequency ($\omega_0 > 0$) reduce the OSR more than adding them at zero frequency.

To the best of our knowledge, zeros at non-zero frequencies have not been used in OLSDM.

The paper is organized as follows: In Section II OLSDM is explained and requirements for input signal amplitude and quantizer bits are derived. In Section III the key component of OLSDM, the modulo integrator, is described in detail, including the effects of finite gain in modulo integrators. The modulo integrator has previously been described in [6], but the effects of finite gain in modulo integrators has not been exhaustively covered.

The modulo resonator is introduced in Section IV. The modulo integrator and modulo resonator are combined in Section V to make a behavioral model of a fifth order low-pass OLSDM with more than 13-bit effective number of bits with an OSR of four. Simulation results from behavioral level models in MATLAB and SPICE are presented in Section V.

II. When is OLSDM equivalent to SDM?

The modulo operator is used extensively in OLSDM to limit the signal swing at the output of modulo integrator. The modulo operator is written as

$$x_r = \langle x \rangle_R \tag{1}$$

where $x \in \langle -\infty, \infty \rangle$ is the input signal, R is the range and $x_r \in \langle -R/2, R/2 \rangle$ is the residue after dividing by the range, R. This modulo function is not the normal mathematical modulo function, but a function that computes the remainder of the input signal after rounding it to an integer number of full scale signal swings (R).

The modulo is similar to what was used in [8] where they proved the equivalence of the open-loop and closed loop representations by symbolic manipulation. The modulo arithmetic used in OLSDM has previously been used in comb filters, as was shown in [9].

The following theorem is useful for the derivations below.

Theorem 1: The modulo of the sum of modulo is equal to the modulo of sum if the range of the two modulus are equal, $R_0 = R_1 = R$

$$\langle \langle x \rangle_{R_0} + \langle y \rangle_{R_0} \rangle_{R_1} = \langle x + y \rangle_R \tag{2}$$

A proof of the theorem is included in Appendix A

The modulo integration, shown in Fig 1, is written as

$$u_n = \left\langle \sum_{i=0}^{\infty} x_{n-i-1} \right\rangle_R \tag{3}$$

where x_n is the input signal to the integrator at time n, u_n is the modulator output signal, and n is the discrete time step. The input signal at time $n-1$ is written as x_{n-1}.

The output of the modulator in Fig. 1 is

$$y_n = \langle u_n - u_{n-1} + q_n - q_{n-1} \rangle_R \tag{4}$$

where q_n is the quantization noise.

Insert (3) in (4) and let $e_n = q_n - q_{n-1}$

$$y_n = \left\langle \left\langle \sum_{i=0}^{\infty} x_{n-i-1} \right\rangle_R - \left\langle \sum_{i=0}^{\infty} x_{n-i-2} \right\rangle_R + e_n \right\rangle_R \tag{5}$$

With (2) (5) reduces to

$$y_n = \langle x_{n-1} + e_n \rangle_R \tag{6}$$

The discrete time equation for a first order low-pass sigma-delta modulator is

$$y_n = x_{n-1} + q_n - q_{n-1} \tag{7}$$

Equation (6) is equal to (7) if

$$|x_n + e_n| < R/2 \tag{8}$$

The absolute value of the filtered quantization noise ($|e_n|$) has a maximum value of one LSB (Least Significant Bit), since $|q_n| \leq 1/2LSB$ and $e_n = q_n - q_{n-1}$. Here $LSB = R/2^B$, where B is the number of bits in the quantizer.

The input signal for first order open-loop sigma-delta modulator must be limited by

$$|x_n| < R/2 - 1LSB = R(1/2 - 1/2^B) \tag{9}$$

We will derive the general input signal limitations for N-order OLSDM, but to reduce the length of equations we define

$$f_{x,n} = \sum_{i=0}^{\infty} x_{n-i} \tag{10}$$

and from (2)

$$\langle \langle f_{x,n} \rangle_R - \langle f_{x,n-1} \rangle_R + e_n \rangle_R = \langle x_n + e_n \rangle_R \tag{11}$$

For second order OLSDM (Fig. 2) the output of the first integrator is

$$u_n = \langle f_{x,n-1} \rangle_R \tag{12}$$

and the output of the second integrator is

$$u_{1,n} = \langle f_{u,n-1} \rangle_R \tag{13}$$

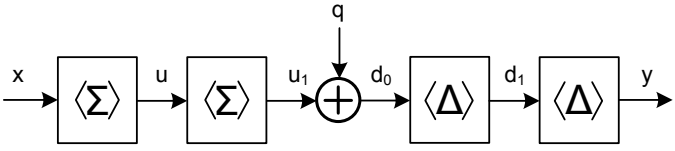

Fig. 2. Second order low-pass open-loop sigma-delta modulator

The quantized signal is

$$d_{0,n} = \langle f_{u,n-1} \rangle_R + q_n \tag{14}$$

And the output signal of the first modulo differentiator is

$$d_{1,n} = \langle \langle f_{u,n-1} \rangle_R - \langle f_{u,n-2} \rangle_R + e_n \rangle_R \tag{15}$$

which by (11) is written as

$$d_{1,n} = \langle u_{n-1} + e_n \rangle_R \tag{16}$$

The output signal of the modulator is

$$y_n = \langle \langle f_{x,n-1} \rangle_R - \langle f_{x,n-2} \rangle_R + e_n - e_{n-1} \rangle_R \quad (17)$$

which by (11) is

$$y_n = \langle x_{n-1} + q_n - 2q_{n-1} + q_{n-2} \rangle_R \quad (18)$$

The maximum absolute value of the quantization noise in (18) is

$$|q_n| + |2q_{n-1}| + |q_{n-2}| = 1/2 + 1 + 1/2 = 2 \quad (19)$$

From this it follows that the input signal must be limited by

$$|x_n| < R/2 - 2LSB = R(1/2 - 2/2^B) \quad (20)$$

(20) is sufficient to ensure that the second order OLSDM is equivalent to a second order SDM. It can be shown that for third order OLSDM the requirement is

$$|x_n| < R/2 - 4LSB = R(1/2 - 4/2^B) \quad (21)$$

For N-order OLSDM the input signal must be limited by

$$|x_n| < R(1/2 - 2^{N-1}/2^B) \quad (22)$$

If $B = N$ the input signal limit is not practical since

$$|x_n| < R(1/2 - 2^{N-1}/2^B) = R(1/2 - 1/2) = 0 \quad (23)$$

Accordingly, $B > N$ to ensure that N-order OLSDM is equivalent to N-order SDM. This is equivalent to the quantizer non-overload criteria in SDM proved in [10]. An N-order sigma-delta modulator will not overload the quantizer if the input signal is limited by $|x_n| < R/4$, and $B = N + 1$.

For $B = N + 1$ in (22)

$$|x_n| < R(1/2 - 1/4) = R/4 \quad (24)$$

In the next section we will cover the key component of analog-to-digital OLSDM, the modulo integrator.

III. Modulo integrator

In this section we discuss the implementation of a modulo integrator in behavioral level models, the switched-capacitor implementation, and effects of finite opamp gain in the modulo integrator.

A. Behavior level implementation

The output of the modulo integrator is described by

$$u_n = \left\langle \sum_{i=0}^{\infty} x_{n-i-1} \right\rangle_R \quad (25)$$

In behavioral level models (25) is impractical due to the infinite modulo. In the definition of the modulo (1) the input signal can take any value, $x_n \in \langle -\infty, \infty \rangle$. This requires the modulo integrator to wrap around infinitely many times if the output signal is to be limited by $u_n \in \langle -R/2, R/2 \rangle$. But since the input signal is limited by (22), the infinite modulo is unnecessary. Assume that $|x_n| < R/2$, which by (22) must be true, then the maximum value after integration but before the modulo is limited by $u_{before,n} \in \langle -R, R \rangle$. Fig. 3 shows an example of the output ($u_{before,n}$) before modulo, and after modulo (u_n) for a sinusoidal input signal (x_n). The modulo integrator is implemented by adding or subtracting the range R. The modulo operation can now be defined as

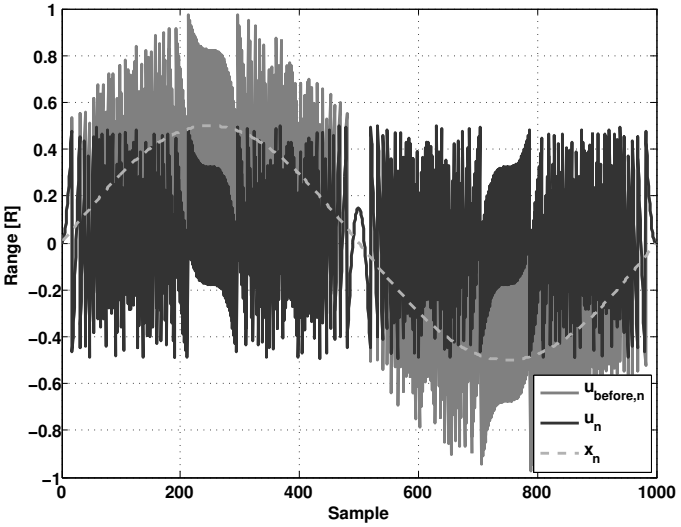

Fig. 3. States of the modulo integrator for a sinusoidal input x_n. The output before modulo is $u_{before,n}$ and the output after is u_n.

$$u_{before,n} = u_{n-1} + x_{n-1} \quad (26)$$

and

$$u_n = \begin{cases} u_{before,n} + R & u_{before,n} \in \langle -R, -R/2] \\ u_{before,n} & u_{before,n} \in \langle -R/2, R/2 \rangle \\ u_{before,n} - R & u_{before,n} \in [R/2, R \rangle \end{cases} \quad (27)$$

The modulo integrator described by (27) can be implemented as a switched-capacitor (SC) circuit [6].

B. Switched-capacitor modulo integrator

The SC modulo integrator is based on the parasitic insensitive integrator shown in Fig. 4. The input signal is sampled at the end of p_1. In p_2 the charge of C_1 is moved to C_2 by forcing node V_x equal to zero with the opamp. The switched-capacitor modulo integrator is shown in Fig. 5. Three clock phases are needed for the modulo integrator, p_1, p_2, and p_3. The clock period is divided into four equally large phases t_0, t_1, t_2, t_3 for a straightforward implementation. Phase one is the combination of the first two phases ($p_1 = t_0 + t_1$), phase

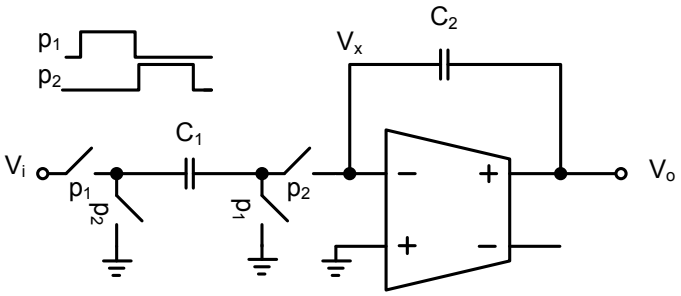

Fig. 4. Parasitic insensitive switched-capacitor integrator

two is the combination of the last two phases ($p_2 = t_2 + t_3$), and phase three is equal to the last phase ($p_3 = t_3$).

The input signal V_i is sampled across capacitor C_1 during p_1. In p_2 the charge across C_1 is moved to C_2. In p_3 the two comparators in Fig. 5 determine whether the output V_o exceeds the references (V_{REF} and $-V_{REF}$), here $|V_{REF}| = R/2$. Capacitor C_3 has been pre-charged in p_1 to $V_{REF} - -V_{REF} = R$.

If the output voltage is larger than V_{REF} C_3 is connected to V_x such that a charge equal to R is subtracted from C_2. If the output voltage is less than $-V_{REF}$ a charge equal to R is added to the charge of C_2. The charge transfer equations for Fig. 5 are (28) if $V_{o,p_2} \in \langle -V_{REF}, V_{REF}\rangle$, (29) if $V_{o,p_2} \in \langle -V_R, V_{REF}]$ and (30) if $V_{o,p_2} \in [V_{REF}, V_R\rangle$.

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} \tag{28}$$

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} + C_3 V_R \tag{29}$$

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} - C_3 V_R \tag{30}$$

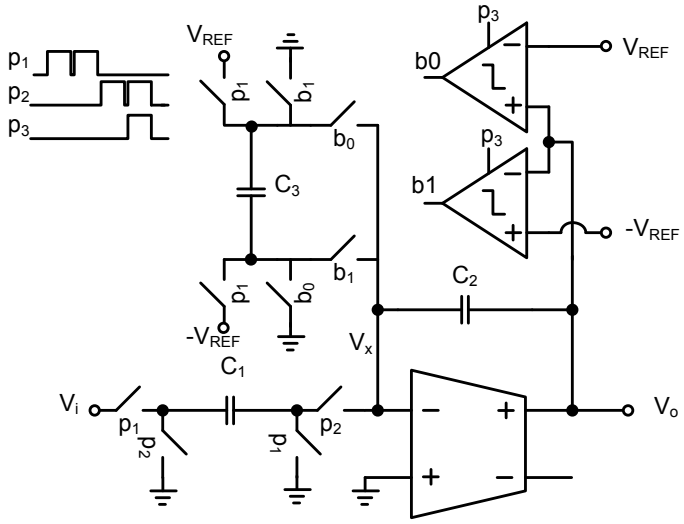

Fig. 5. Switched-capacitor modulo integrator

If $C_1 = C_2 = C_3$ the charge transfer equations implement the modulo defined in (27). The modulo operation ensures that the output signal in p_3 stays within $V_o \in \langle -V_R/2, V_R/2\rangle$ as long as $V_i \in \langle -V_R/2, V_R/2\rangle$.

C. Effects of finite gain in modulo integrators

One of the non-idealities in SC integrators is the finite opamp gain. The effects of finite opamp gain was covered in [11] and [12]. The transfer function of an integrator with finite gain can be approximated by

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}\frac{az^{-1}}{1 - bz^{-1}} \tag{31}$$

where

$$a = 1 - \frac{1 + C_1/C_2}{A_0} \tag{32}$$

$$b = 1 - \frac{1}{A_0} \tag{33}$$

and A_0 is the DC gain of the opamp. The derivation is included in Appendix B. A block model of the modulo integrator is shown in Fig. 6.

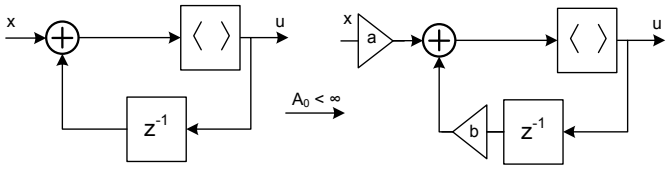

Fig. 6. Block model of the modulo integrator for finite DC gain.

We have assumed that the modulo operation does not influence the effects of finite gain. To verify the model in Fig. 6 it is implemented in SIMULINK and compared with two other models, one based on the difference equations and one based on a SPICE implementation.

An expression can be derived for the output of a first-order OLSDM using the modulo arithmetic used in Section II. The output of a first order OLSDM with finite DC gain in the modulo integrators can be approximated by the difference equation

$$y_n = \left\langle x_{n-1} - \frac{q_{u,n}}{A_0} + q_n - q_{n-1} \right\rangle_R \tag{34}$$

where $q_{u,n}$ is a white noise approximation of the modulo integrator output u_n. The derivation is left for Appendix C.

The difference between (34) and (6) is the term $-q_{u,n}/A$. Due to the finite opamp gain there is a leakage of u_n to the output. The modulo integrator output (u_n) is a deterministic signal of the input, but we assume it can be approximated as quantization noise with the limits $q_{u,n} \in \langle -R/2, R/2\rangle$.

From (34) the *signal-to-noise and distortion ratio* (SNDR) can be calculated. For a sinusoidal input the SNDR is

$$SNDR = 10log\left(\frac{A^2/2}{\frac{1}{12A_0^2 OSR} + \frac{LSB^2}{12} \times K}\right) \tag{35}$$

where A is the amplitude of the sinusoid, the first term in the denominator is the effects of finite gain, and the second term the quantization noise where $K = 2\int_0^{f_s/2OSR} |NTF(z = e^{j\omega})|^2 df$. The calculation of (35) is left for Appendix D. With $B = 7$, $OSR = 4$ and $A_0 = 50dB$ the expected SNDR is 51.3-dB.

An FFT of the SIMULINK model (Fig. 6) is shown in Fig. 7. Fig. 8 shows the FFT of the approximate model as defined by (34). The FFT of the SPICE model output is shown in Fig. 9.

The approximation in Fig. 8 is different from the others, here the noise floor is relatively flat up to $0.01f_s$. At that point the shaped quantization noise is larger than the leakage

from the integrator output (from (34)) and we get the high-pass noise shaping.

For both the SIMULINK model in Fig. 7 and SPICE model in Fig. 9 we can see that the contribution $q_{u,n}/A_0$ is not white, but equal to u_n/A_0. Fig. 10 shows the FFT of the modulo integrator output (u_n) from the SIMULINK simulations.

The vertical line in the figures denote the upper bandwidth limit for noise calculation. As a quick estimate of the performance (35) works well. It overestimates the effects of noise and has an SNDR of 51.3-dB compared to 52.2-dB for the SIMULINK model, 51.66-dB in the SPICE model and 51.44-dB for the approximation (34). These models show that the modulo operation does not significantly influence the equations for the effects of finite gain.

Calculation speed is very different in the three models. Calculating (35) takes less than a second, while the SIMULINK model take ten seconds for 2^{15} points, and the SPICE simulations take a thousand seconds for 2^{15} points.

To increase the resolution of this first order low-pass OLSDM we can either increase the quantizer resolution, which we will not do, or reduce the in-band quantization noise with higher order noise shaping. To get higher order noise shaping we can increase the number of zeros in the noise transfer function (NTF) of the modulator. Either at z=1 (zero frequency) with modulo integrators, or introduce zeros at non-zero frequencies. The next section introduce the modulo resonator, which is used to insert a zero at a non-zero frequency in the noise transfer function.

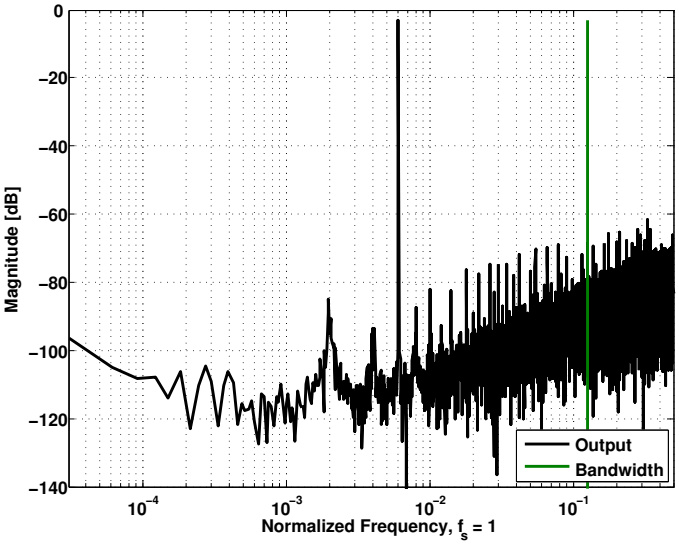

Fig. 7. SIMULINK model, SNDR = 52.20-dB

IV. Modulo resonator

Zeros at non-zero frequency in the noise transfer function reduce the oversampling ratio for a given quantizer resolution. With zeros at non-zero frequency one can implement band-pass sigma-delta modulators. In this section the modulo resonator is introduced and the ideal and simulated performance is discussed.

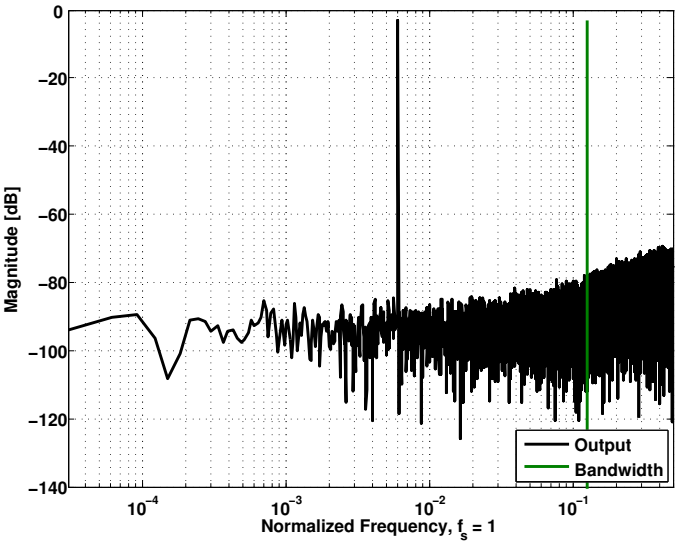

Fig. 8. Approximation, SNDR = 51.44-dB

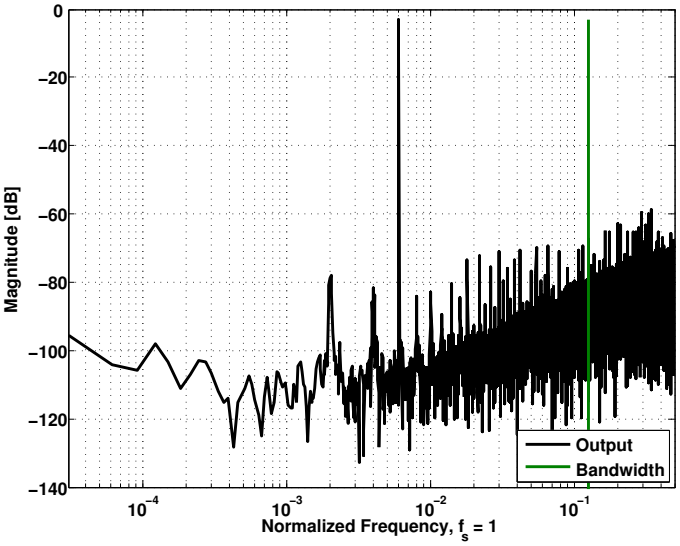

Fig. 9. SPICE model, SNDR = 51.66-dB

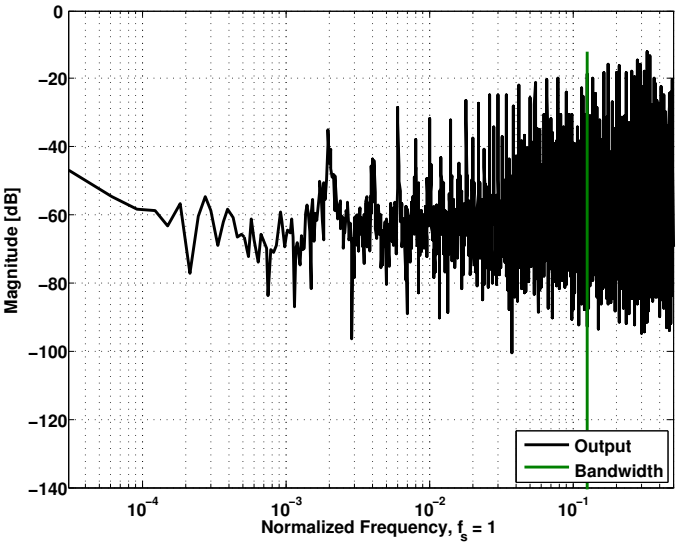

Fig. 10. FFT of u_n

A model of modulator with zeros at non-zero frequency can be seen in Fig. 11. In a world without signal swing limitations the input signal (x_n) can be conditioned with a resonator, the output of the resonator quantized, and input signal restored with a notch filter. The quantization noise will pass through the notch filter and be filtered accordingly. The output of the modulator is written as

$$Y(z) = STF(z)X(z) + NTF(z)Q(z) \tag{36}$$

$STF(z)$ is the signal transfer function and $NTF(z)$ is the noise transfer function.

The input signal pass through unchanged if the notch filter response matches the resonator response, thus $STF(z) = 1$.[2]

In Fig. 11 the $NTF(z)$ is equal to the notch filter response, which has a zero at a non-zero frequency.

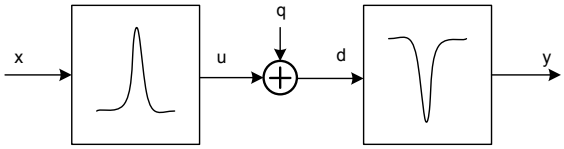

Fig. 11. Ideal open-loop implementation of NTF zeros at non-zero frequency

A common resonator used in sigma-delta modulators is based on the lossless discrete integrator (LDI) [13] shown in Fig. 12. The LDI resonator has a pair of complex conjugate poles at

$$z_p = \rho \pm j\sqrt{(1-\rho^2)}, \rho = 1 - g/2 \tag{37}$$

and a resonance frequency of $\omega_0 = cos^{-1}(\rho)$. The advantage of the LDI is the tunable resonance frequency.

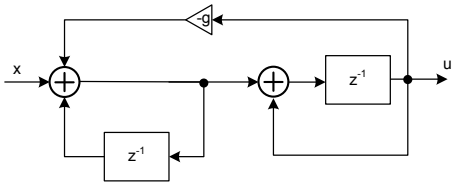

Fig. 12. Resonator based on the lossless discrete integrator (LDI)

If the integrators in Fig. 12 are replaced with modulo integrators we get the modulo resonator shown in Fig. 13. With this modulo resonator we can implement Fig. 11 as shown in Fig. 14. Fig. 14 is a modulo resonator followed by a linear quantizer and a modulo notch filter. The modulo operations at the end of the notch filter reverse the modulo in the resonator.

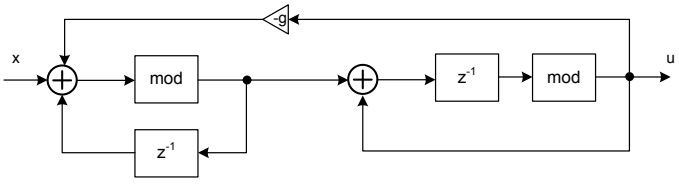

Fig. 13. The modulo resonator

[2]The $STF(z)$ will probably also contain a time delay, depending on the implementation, $STF(z) = z^{-n}$

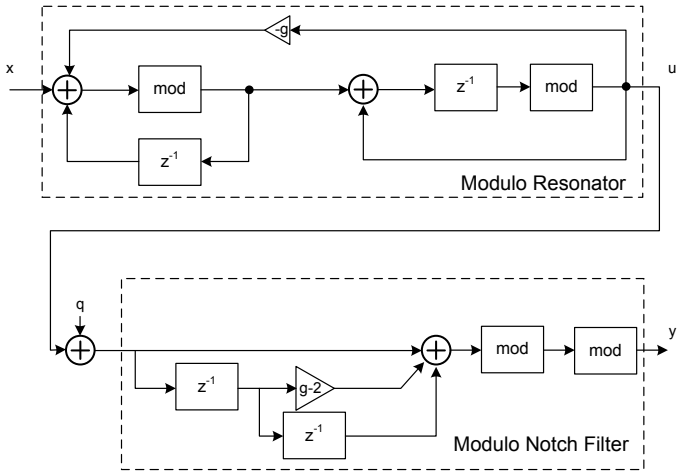

Fig. 14. The open-loop sigma-delta modulator with NTF zeros at non-zero frequency

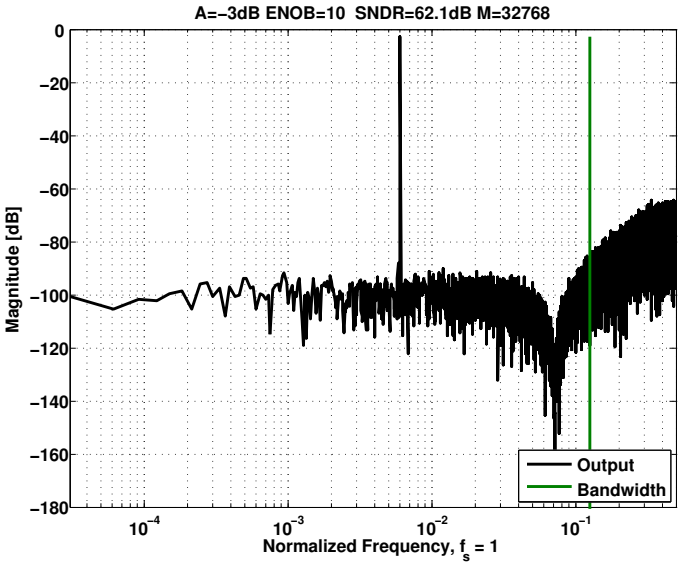

Fig. 15. Modulator response. Magnitude of a 2^{15} point FFT. Input signal amplitude is -3dBFS, input signal frequency is at $f_i = 0.006$ with a normalized sampling frequency, $f_s = 1$. The SNDR with $OSR = 4$ is 62.1-dB

The noise transfer function of the modulator in Fig. 14 is

$$NTF(z) = z^2 + (g-2)z + 1 \tag{38}$$

And has an ideal SNDR of

$$SNDR = 10log\left(\frac{A^2/2}{2\int_0^{f_s/2OSR} Q_M^2(f)|NTF(z)|^2 df}\right) \tag{39}$$

if we assume sinusoidal input. Here $Q_M^2(f)$ is the power spectral density of the quantization noise given by

$$Q_M^2(f) = \frac{LSB^2}{12f_s} = \frac{1}{2^{2B}12f_s} \tag{40}$$

where $LSB = R/2^B$ and $R = 1$.

The optimum zero frequency can be calculated from (39). Using an OSR of four the optimum zero frequency is $f_i = 0.0718f_s$ ($g = 0.2$).

Fig. 14 was implemented as a SIMULINK model. Fig. 15 is a 2^{15} point FFT of the modulator output (y_n) with an input signal amplitude of $-3dBFS$ and a quantization noise power equivalent to a 7-bit quantizer. Coherent sampling and a Hanning window was used to avoid spectral leakage of the signal power into neighboring FFT bins. A brick-wall filter with bandwidth from $0 - f_s/2OSR$ was used to calculate the SNDR. The vertical line in Fig. 15 denotes the bandwidth.

For $f_s = 1$, $OSR = 4$, $B = 7$, $A = 1/\sqrt{8}$ the ideal SNDR from (39) is 62-dB. The simulated SNDR match the ideal SNDR (1% difference).

A. Effects of finite gain in modulo resonators

Exact analysis of the effects of finite gain in a modulator with a modulo resonator is complex. The derivation is left for Appendix E.

The modulator output (y_n in Fig. 14) with finite gain in the modulo resonators can be approximated by

$$y_n \approx \langle x_{n-1} + (1+g)\epsilon_{p,n-1} + e_n \rangle_R \tag{41}$$

where ϵ_p is the leakage from the first modulo integrator. The shaped quantization noise is represented by e_n. The leakage from the first modulo integrator dominate over the leakage from the second modulo integrator if the opamp gains in the two integrators are equal.

With (41) the SNDR is

$$SNDR \approx 10log\left(\frac{A^2/2}{\frac{(1+g)^2}{12A_0^2}\frac{1}{OSR} + \frac{LSB^2}{12} \times K}\right) \tag{42}$$

where $K = \int_0^{f_s/2OSR} |NTF(z)|^2 df$.

Accuracy of (42) depend on the DC gain. It overestimates the SNDR with 1.5-dB to 1-dB for a DC gain of 60-dB - 80-dB compared to the derivation in Appendix E. But the leakage from the modulo integrator is approximated by a white noise source, which has higher power than the power of the actual leakage. Accordingly, the two assumptions: leakage approximated by a white noise source, and assuming ϵ_p is the dominating noise source, work in opposite directions.

For $A = -3dBFS$, $OSR = 4$, $g = 0.2$, $LSB = 1/2^7$ and a DC gain of 60-dB, the approximate SNDR from (42) is 59.5-dB. Whereas for 40-dB DC gain the SNDR is 43.1-dB.

Using the previously described modulo integrators in a SIMULINK model of the modulator from Fig. 14, the SNDR is 59.2-dB for 60-dB DC gain and 42.5-dB for 40-dB DC gain. A difference of 0.3-dB (4%) at 60-dB DC gain and 0.6-dB (7%) at 40-dB DC gain.

V. Fifth-order low-pass OLSDM

It has previously been shown that the accuracy of SC circuits depend on the capacitor mismatch, finite DC gain and unity-gain bandwidth of the opamp [11], [12]. We have discussed the effects of finite DC gain, but left the derivation of capacitor mismatch and finite unity-gain bandwidth for later work. But we expect the effects to be similar and limit the performance to below 14-bit ENOB. This assumes no calibration or trimming.

Stages in an OLSDM can be pipelined and it is possible to use high latency quantizers such as pipelined ADCs or SAR ADCs. One in envisioned application of OLSDM is a 14-bit high speed (20MS/s) ADC. In this section we describe a fifth-order OLSDM with an OSR of four and 13-bit ENOB.

A. Ideal modulator

The modulator is seen in Fig. 16. It has two modulo resonators, a modulo integrator, a 7-bit quantizer, a modulo differentiator, and two modulo notch filters. To ensure that (22) is satisfied a gain of 0.9 is inserted between the first and second resonators, and between the second resonator and the modulo integrator (this is not shown in Fig. 16).

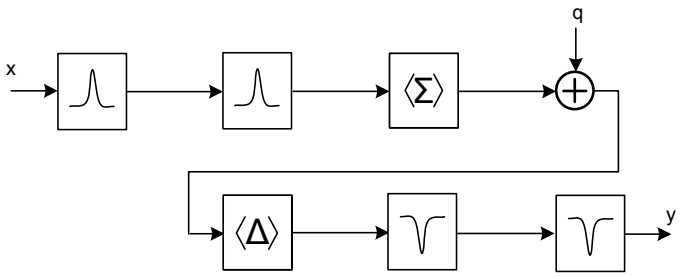

Fig. 16. Fifth-order open-loop sigma-delta modulator

The noise transfer function of the modulator in Fig. 16 is given by

$$NTF(z) = \frac{(z^2 + (g_1 - 2)z + 1)(z^2 + (g_2 - 2)z + 1)(z - 1)}{0.81} \tag{43}$$

And the ideal SNDR can be calculated with (39), using the NTF from (43). With an OSR of four the optimal constants are $g_1 = 0.17$ and $g_2 = 0.48$. For $OSR = 4$, $A = -3dBFS$ and $B = 7$ the ideal SNDR is 85-dB.

A 2^{15} point FFT is calculated from the output of a MATLAB simulation of the ideal modulator in Fig. 16. The FFT is shown in Fig. 17. The simulated match the ideal SNDR (1% difference).

The input signal must be limited as stated in (22). An input signal amplitude of -3dBFS $= 1/\sqrt{8} \approx 0.354$ is used in the simulations. If we insert for $N = 5$ and $B = 7$ in the input signal limit (22)

$$|x(n)| < R(1/2 - 2^{5-1}/2^7) = 0.375 \tag{44}$$

Thus the modulator is valid for an input signal amplitude of -3dBFS.

B. Modulator with finite opamp gain in modulo integrators

Fig. 18 shows the fifth order sigma-delta modulator with the the modeled opamp gain. The modulo integrators are modeled with an opamp gain of 85-dB in the first resonator, 75-dB in second resonator, and 65-dB in the last modulo integrator. These gains were chosen from design equations based on (42). Assume the leakage due to finite opamp gain in the first modulo resonator dominate. The SNDR is then estimated from (42). The estimated SNDR for this modulator is 83.3-dB for an input amplitude of -3dBFS. Fig. 19 is a 2^{15} point FFT of

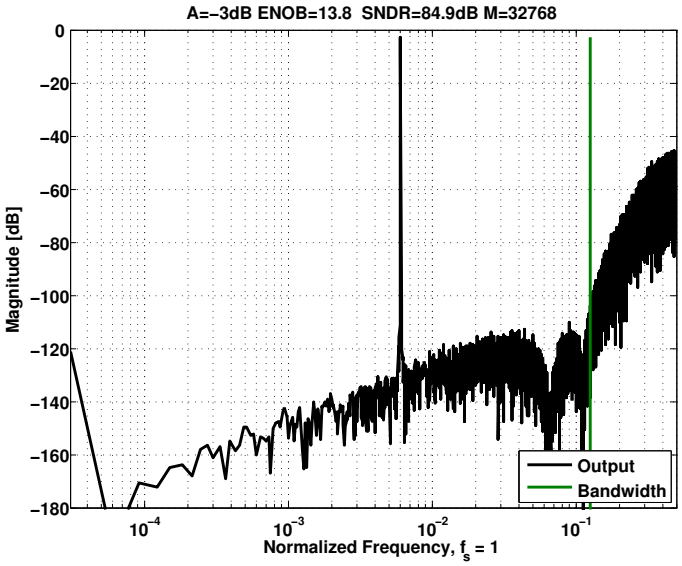

Fig. 17. Modulator output. Magnitude of a 2^{15} point FFT of the modulator output. Input signal amplitude $-3dBFS$. Input frequency $f_i = 0.006$ and sampling frequency $f_s = 1$. With an $OSR = 4$ the SNDR is 84.9-dB

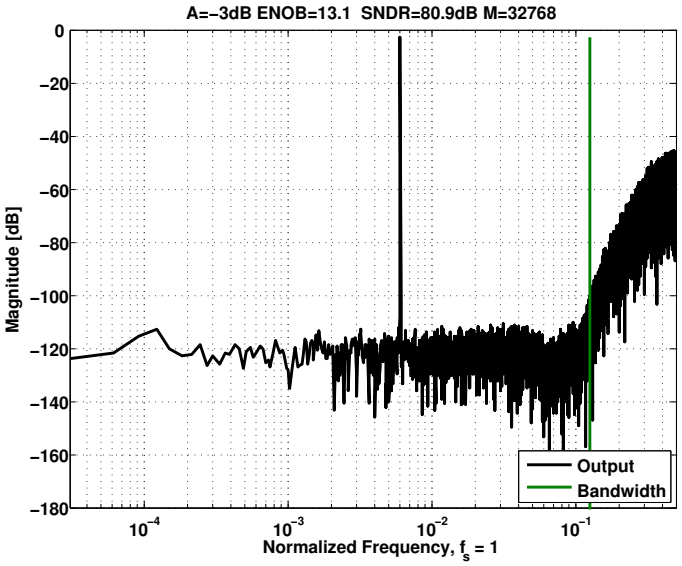

Fig. 19. Magnitude of a 2^{15} point FFT of the modulator output. Input signal amplitude $-3dBFS$, input frequency $f_i = 0.006$ and sampling frequency $f_s = 1$. With an $OSR = 4$ the SNDR=80.9-dB

the modulator output (y_n) using an input signal amplitude of $-3dBFS$.

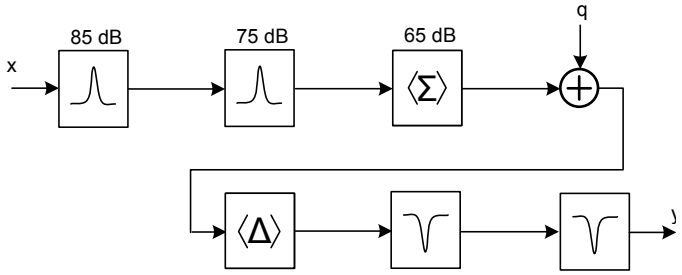

Fig. 18. Fifth-order open-loop sigma-delta modulator. The DC gain of opamps are shown above the stages.

The simulated SNDR is 80.9-dB (13.15-bit ENOB[3]), or 2.4-dB below the estimated SNDR. This is expected due to leakage from later stages. If we increase the DC gain in the second modulo resonator and the last modulo integrator to 200-dB, we remove them as noise contributors. This increases the SNDR to 82.8-dB, which is 0.5-dB (6%) lower than the estimated.

The modulator in Fig. 19 was implemented in SPICE as a switched capacitor circuit.

C. SC modulator

Fig. 20 shows the switched-capacitor implementation of the modulator. A single ended modulator was used for simplicity.

The opamps have a DC gain of 85-dB, 85-dB, 75-dB, 75-dB, and 65-dB The opamp was implemented as a macro-model of a single-pole operational amplifier.

A comparison between the MATLAB model and the SPICE model is shown in Fig. 20, here a 2^{15} point FFT was run on both the SPICE and the MATLAB outputs. The SNDR is

[3]ENOB = (SNDR-1.76)/6.02

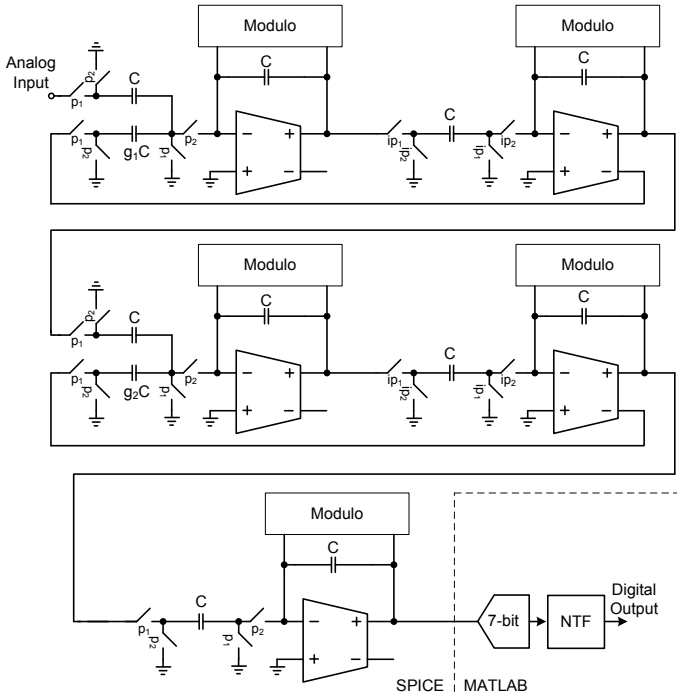

Fig. 20. Fifth order OLSDM SPICE model. Quantization and NTF are implemented in MATLAB

the same for both models. In SPICE, however, there is more harmonic content, with the second harmonic visible in the FFT.

The quantizer and NTF for the SPICE simulations is implemented in MATLAB. A 7-bit ideal quantizer is used instead of the linear approximation to quantization noise.

VI. Conclusion

In this paper we introduced the modulo resonator for open-loop sigma-delta modulators (OLSDM). It was used with a modulo notch filter to introduce a zero in the noise transfer

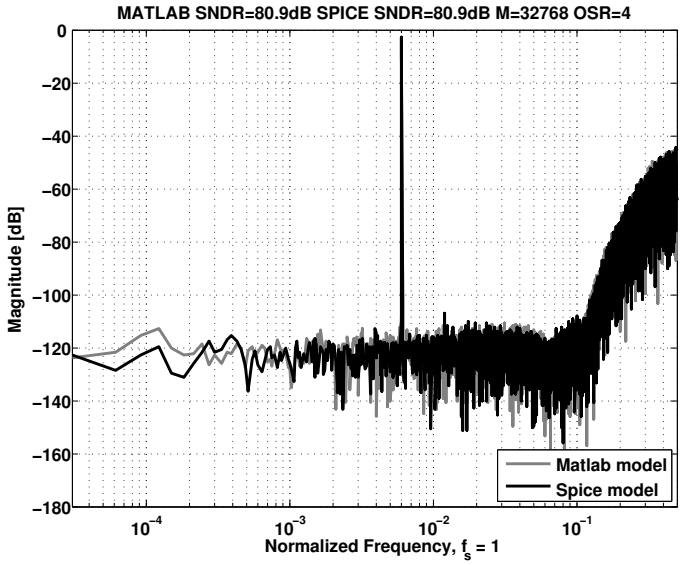

Fig. 21. Comparison of SPICE model and MATLAB model. Input signal amplitude $-3dBFS$, input frequency $f_i = 0.006$ and sampling frequency $f_s = 1$. With an $OSR = 4$ the SNDR is 80.9-dB for the MATLAB model and 80.9-dB for the SPICE model.

function at a non-zero frequency. The modulo resonator and previously published modulo integrator were used in a behavioral model of a switched-capacitor fifth-order OLSDM with more than 13-bit effective number of bits for an oversampling ratio of four. We proved that the number of bits in the quantizer (B) must be larger than the order of the modulator (N) to ensure equivalence between OLSDM and sigma-delta modulation.

APPENDIX A
PROOF OF MODULO THEOREM

Proof: From definition

$$\langle a + nR \rangle_R = \langle a \rangle_R \tag{45}$$

where n is an integer. Given

$$\langle \langle x \rangle_R + \langle y \rangle_R \rangle_R \tag{46}$$

we can write $\langle x \rangle_R = x - nR$ and $\langle y \rangle_R = y - mR$, where n and m are integers. From (45) it follows that

$$\langle x - nR + y - mR \rangle_R = \langle x + y \rangle_R \tag{47}$$

■

APPENDIX B
EFFECTS OF FINITE GAIN IN SC INTEGRATORS

If we assume infinite DC gain in the opamp the charge transfer equation is simply

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} \tag{48}$$

The z-domain transfer function of (48) is

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \tag{49}$$

If $C_1 = C_2$ (49) is the well known transfer function of a discrete time integrator and is a good approximation if the DC gain (A_0) is much higher than the accuracy required. If the DC gain is close to, or lower than the accuracy (49) no longer apply.

With finite opamp gain the voltage V_x (in Fig. 4) will be different from zero. A non-zero V_x will result in a residual charge on capacitor C_1 given by $Q_{1,n} = C_1 V_x$. The charge transfer equation change into

$$Q_{2,n} = Q_{2,n-1} + Q_{1,n-1} + Q_{1,n} \tag{50}$$

where $Q_2 = C_2(V_o - V_x)$, $Q_{1,n-1} = C_1 V_i$. The residual voltage V_x is equal to $V_x = -V_o/A_0$. We define

$$\alpha = 1 + \frac{1}{A_0} \tag{51}$$

If we expand (50) we get

$$\alpha V_{0,n} = \alpha V_{o,n-1} + \frac{C_1}{C_2} V_{i,n-1} - \frac{C_1}{C_2} \frac{V_{o,n}}{A_0} \tag{52}$$

Solved for V_o/V_i and transferred to the z-domain we get the transfer function

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{\left(\dfrac{1}{1 + \dfrac{1 + C_1/C_2}{A_0}} \right) z^{-1}}{1 - \alpha \left(\dfrac{1}{1 + \dfrac{1 + C_1/C_2}{A_0}} \right) z^{-1}} \tag{53}$$

If we assume $A_0 >> 1$ (53) can be approximated to first order by

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{\left(1 - \dfrac{1 + C_1/C_2}{A_0} \right) z^{-1}}{1 - \left(1 - \dfrac{1}{A_0} \right) z^{-1}} \tag{54}$$

APPENDIX C
EFFECTS OF FINITE GAIN IN MODULO INTEGRATORS

From charge transfer equations the output of the modulo integrator is

$$\alpha u_n = \langle \alpha u_{n-1} + x_{n-1} - u_n/A_0 \rangle_R \tag{55}$$

where $\alpha = 1 + 1/A_0$ and A_0 is the DC gain of the opamp. We also have

$$\alpha u_{n-1} = \langle \alpha u_{n-2} + x_{n-2} - u_{n-1}/A_0 \rangle_R \tag{56}$$

and that

$$\alpha u_{n-2} = \langle \alpha u_{n-3} + x_{n-3} - u_{n-2}/A_0 \rangle_R \tag{57}$$

Using (2) the output of the modulo integrator is

$$\begin{aligned} u_n &= \frac{\left\langle \sum_{i=0}^{\infty} x_{n-1-i} \alpha^i - \sum_{i=0}^{\infty} \dfrac{u_{n-i}}{A_0} \alpha^i \right\rangle_R}{\alpha} \\ &= \left\langle \sum_{i=0}^{\infty} x_{n-1-i} \alpha^{i-1} - \sum_{i=0}^{\infty} \frac{u_{n-i}}{A_0} \alpha^{i-1} \right\rangle_R \end{aligned} \tag{58}$$

The output of the modulator is

$$y_n = u_n - u_{n-1} + q_n - q_{n-1} \tag{59}$$

using (2) and (58)

$$y_n = \left\langle \frac{x_{n-1}}{\alpha} - \frac{u_n}{A_0\alpha} + q_n - q_{n-1} \right\rangle_R \tag{60}$$

Assuming $A_0 >> 1$ we can approximate the modulator output by

$$y_n = \left\langle x_{n-1} - \frac{u_n}{A_0} + q_n - q_{n-1} \right\rangle_R \tag{61}$$

The signal u_n can be written as (25). This signal is the quantization noise after rounding the integrator output to the range R. We assume this quantization noise is white. Assume $u_n \approx q_{u,n} \in \langle -R/2, R/2 \rangle$. Then (61) simplifies to

$$y_n = \left\langle x_{n-1} - \frac{q_{u,n}}{A_0} + q_n - q_{n-1} \right\rangle_R \tag{62}$$

Appendix D
Calculation of the SNDR

The power spectral density of quantization noise is given by the well known equation

$$Q^2(f) = \frac{LSB^2}{12 f_s} \tag{63}$$

where f_s is the sampling frequency. For a given bandwidth the noise power is

$$Q^2 = 2\int_0^{f_s/2OSR} Q^2(f)df = \frac{LSB^2}{12}\frac{1}{OSR} \tag{64}$$

The LSB of $q_{u,n}/A_0$ can be written as R/A_0. And if we assume $R = 1$ the noise power of the modulo integrator output leakage is given by

$$Q_u^2 = \frac{1}{12 \times A_0^2}\frac{1}{OSR} \tag{65}$$

The quantization noise in a first order OLSDM is high-pass filtered, and has a noise transfer function of

$$NTF(z) = 1 - z^{-1} \tag{66}$$

The LSB of the quantization noise is $LSB = R/2^B$, so with $R = 1$ the quantization noise power can be calculated from

$$Q_n^2 = 2\int_0^{f_s/2OSR} \frac{1}{12 \times 2^{2B} f_s} |NTF(z = e^{j\omega})|^2 df \tag{67}$$

The signal to noise and distortion ratio can be written as

$$SNDR = 10log\left(\frac{A^2/2}{Q_u^2 + Q_n^2}\right) \tag{68}$$

and inserted for (65) and (67) gives

$$SNDR = 10log\left(\frac{A^2/2}{\frac{1}{12A_0^2 OSR} + \frac{LSB^2}{12} \times K}\right) \tag{69}$$

where

$$K = 2\int_0^{f_s/2OSR} |NTF(z = e^{j\omega})|^2 df \tag{70}$$

Appendix E
Effects of finite gain in modulo resonators

We start with the difference equations for the output of the integrators in the modulo resonator. And we assume that the modulo has no effect. The output of the first modulo integrator is given by

$$\alpha p_n = (1+g)\alpha p_{n-1} + x - g u_n - \epsilon_p \tag{71}$$

where $\epsilon_p = p_u/A_0 \approx q_p/A_0$ is the leakage as described earlier for modulo integration and $\alpha = 1 + 1/A_0$, where A_0 is the DC gain. The leakage is now $(1+g)$ larger than for a single modulo integrator, which is due to the feedback capacitor given by gC in Fig. 20. The feedback capacitor increase the residual charge since the voltage V_x in the modulo integrator is now forced across a larger capacitance $C + gC$. The output of the modulo resonator is written as

$$\alpha u_n = \alpha u_{n-1} + p_{n-1} - \epsilon_u \tag{72}$$

where $\epsilon_u = u_n/A_0 \approx q_u/A_0$ is the leakage from the second modulo integrator. Transferring to the z-domain and solving the equations for u we get

$$U(z) = \frac{xz^{-1}}{B(z)} - \frac{(1-z^{-1})\alpha\epsilon_u}{B(z)} - \frac{(1+g)\epsilon_p z^{-1}}{B(z)} \tag{73}$$

where $B(z)$ is

$$B(z) = \alpha^2 z^{-2} + (g - 2\alpha^2)z^{-1} + \alpha^2 \tag{74}$$

After the modulo resonator the signal is quantized and filtered by the notch filter. The notch filter transfer function is equal to the noise transfer function. The NTF can be written as[4]

$$NTF(z) = z^{-2} + (g-2)z^{-1} + 1 \tag{75}$$

and we see that if $\alpha = 1$ then $NTF(z) = B(z)$.

The output of the modulator will be

$$Y(z) = U(z) \times NTF(z) + Q(z) \times NTF(z) \tag{76}$$

inserted for (73) in (76)

$$Y(z) = \frac{NTF(z)}{B(z)}\left[xz^{-1} + (1-z^{-1})\alpha\epsilon_u + (1+g)\epsilon_p z^{-1}\right] + Q(z) \times NTF(z) \tag{77}$$

There are three effects that can be seen from (77). The leakage from the first integrator ϵ_p leaks directly to the output scaled by a factor $1 + g$. The leakage from the second integrator, ϵ_u, is first order high pass filtered. The finite gain in the modulo integrators cause an incomplete pole/zero cancellation between the NTF(z) and B(z), for low DC gain this will increase the noise contribution. For high DC gain we can assume that $\alpha \approx 1$ such that $NTF/B(z) \approx 1$. Then (77) becomes

$$Y(z) = X(z)z^{-1} + (1-z^{-1})\epsilon_u + (1+g)\epsilon_p z^{-1} + Q(z) \times NTF(z) \tag{78}$$

[4]Here we have shifted the NTF in time by multiplying by z^{-2}

Transferred back to time domain we have the difference equation

$$y_n = \langle x_{n-1} + \epsilon_{u,n} - \epsilon_{u,n-1} + (1+g)\epsilon_{p,n-1} + e_n \rangle_R \quad (79)$$

where e_n is the shaped quantization noise.

The dominating noise source in (79) is the the leakage from the first integrator ($(1+g)\epsilon_{p,n-1}$). The modulator output can thus be approximated by

$$y_n \approx \langle x_{n-1} + (1+g)\epsilon_{p,n-1} + e_n \rangle_R \quad (80)$$

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