Design and behavioral simulation of comparator based switched-capacitor circuits

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Outline

- Motivation
- Comparator based switched capacitor circuits
- Design equations
- Example of a comparator-based switched-capacitor circuit
- Future work

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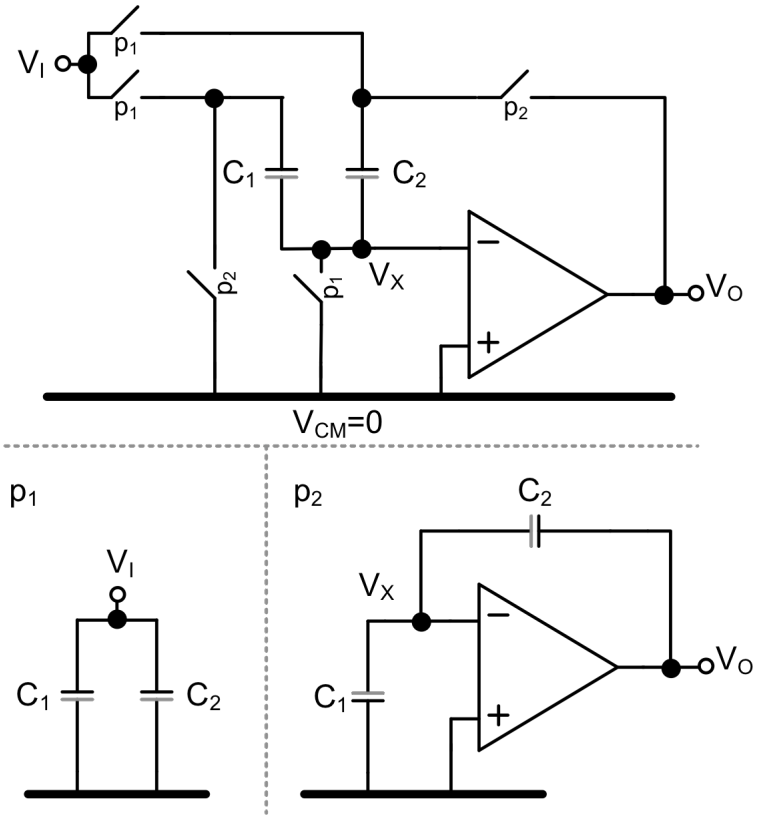
Motivation: Why CBSC

Conventional switched-capacitor amplifier



- An amplifier used in pipelined ADCs
- In nano-scale technologies (< 100nm) the supply voltage and transistor output resistance is low.
- Harder to design efficient high-gain (>40dB) OTAs
- Is there an alternative to OTA based switched-capacitor?

$$H_0(z) = 1 + \frac{C_1}{C_2} z^{-1} \xrightarrow{\text{Finite OTA gain}} H_1(z) = H_0(z) \times \frac{1}{1 + \frac{H_0(1)}{A}}$$

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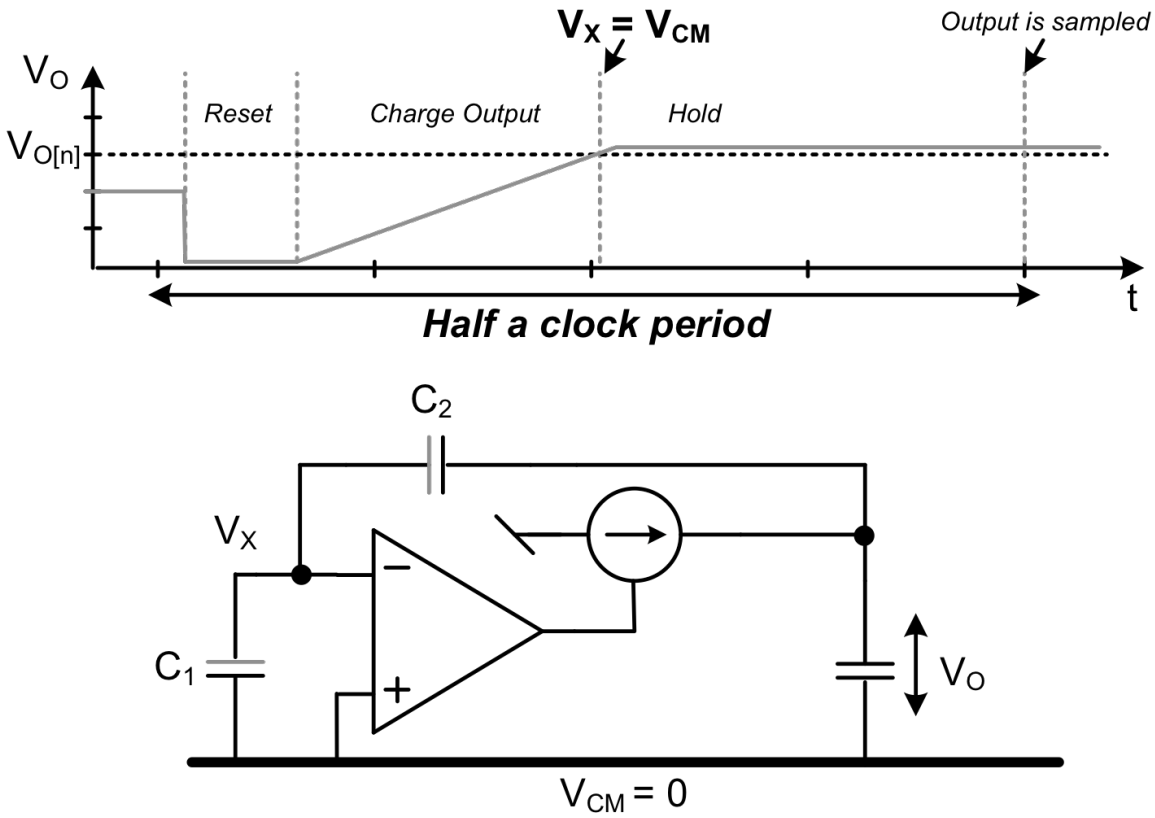
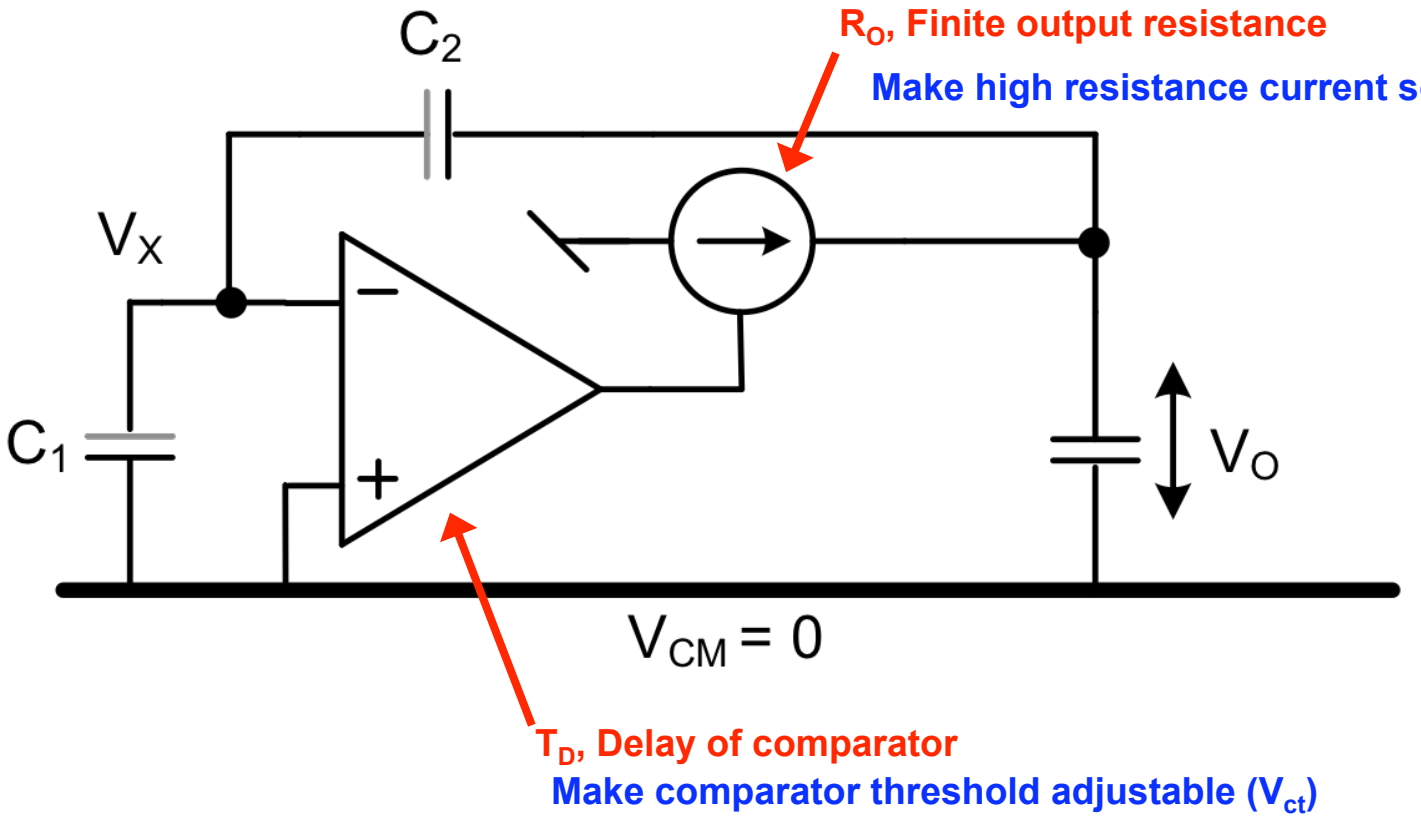
Comparator-based switched capacitor circuits



- Introduced in [1]
- OTA replaced by current source and comparator
- Detects virtual ground
- Easier to make high impedance current sources and a fast comparator than a OTA
- An OTA needs to be stable in a feedback loop, a comparator does not

Non-ideal effects



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The design equations

- **With these two effects the output voltage of the CBSC amplifier is**

$$V_O = 2e^{\frac{-T_d}{R_O C_O}} + I_O R_O \left[1 - e^{\frac{-T_d}{R_O C_O}} \left(1 + 2\frac{V_{ct}}{I_O R_O} \right) \right]$$

Gain of amplifier

Overshoot caused by comparator delay

1. Required sampling capacitor (from [2])

$$C = a_1 \frac{48kT2^{2B}}{V_{pp}^{\ 2}}$$

2. Necessary current

$$I_O = C_o \frac{(V_{pp}/4 + V_{cm})}{1/2f_s - T_r}$$

3. Required output resistance

$$R_O = \frac{-T_d}{\ln(1-\varepsilon_g)C_O}$$

4. Required comparator threshold

$$V_{ct} = -\tfrac{1}{2} I_O R_O \left(1 - e^{\frac{T_d}{R_O C_O}} \right)$$

Given:
- T_d = Comparator delay
- ε_g = Gain error
- V_{PP} = Peak to peak output voltage
- T = Temperature
- B = Number of bits
- k = Boltzmann's constant
- a_1 = constant
- T_r = reset time
- V_{cm} = Common mode voltage
- f_s = sampling frequency

Calculate:
- I_O = Current in current source
- R_O = Output resistance
- C = Sampling capacitor
- V_{ct} = Comparator threshold

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The example system

Given

Parameter	Value
B	9
T	300K
k	1.38e-23
a_1	3
V_{PP}	1V
V_{CM}	0.6V
ε_g	1/(2^B)
T_d	0.5ns
T_r	1ns
fs	50MHz

Calculated

Parameter	Value
C	160fF
I_O	30µA
R_O	1.1MΩ
V_{ct}	32mV

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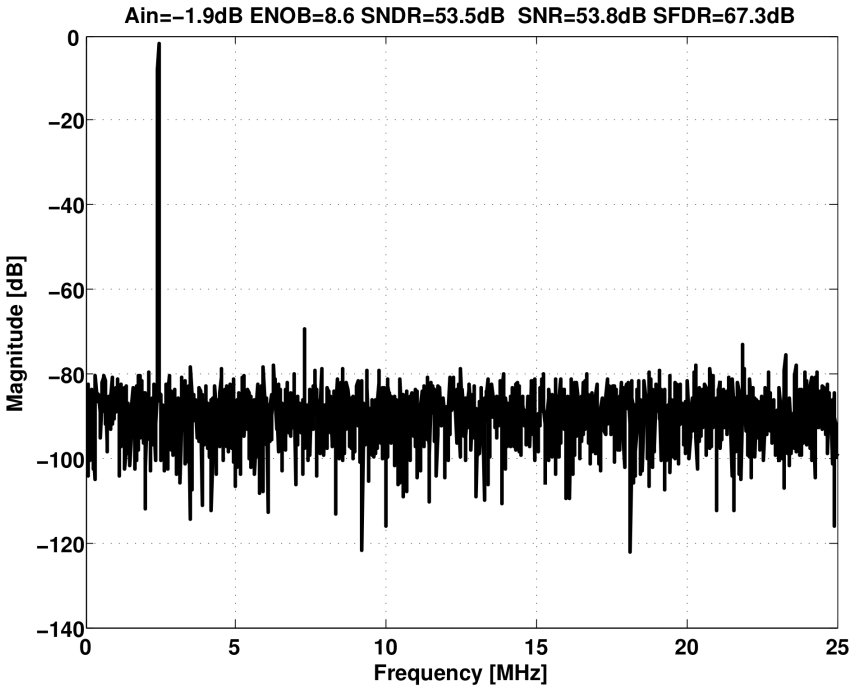
Simulation results

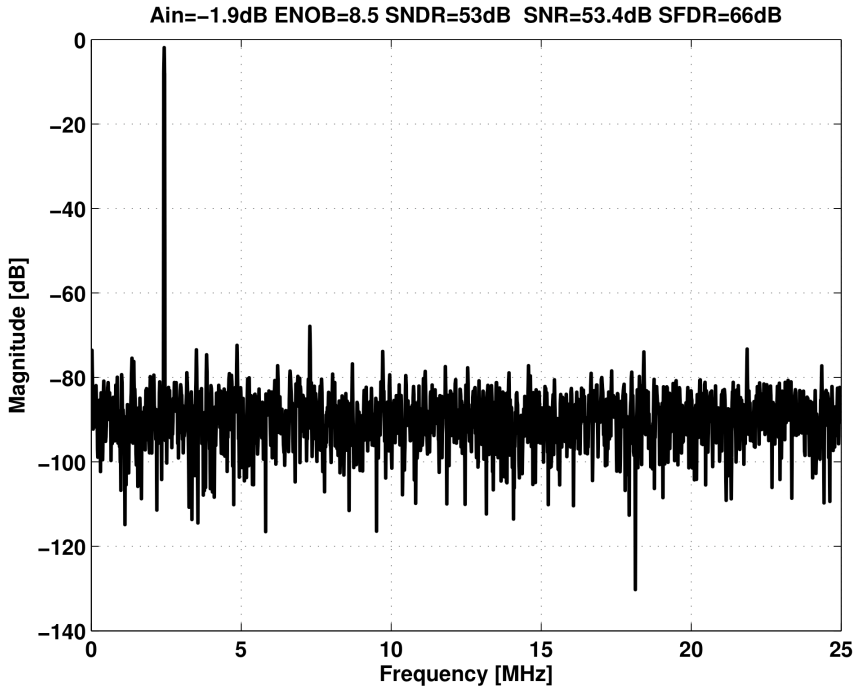
MATLAB MODEL

Design equations



SPICE MODEL

Macro model of real circuit



< 7 % Difference for SNDR and SNR

Both models can be downloaded from http://www.wulff.no/carsten . Tools & Scripts, Behavioral model of comparator-based switched-capacitor circuits

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Conclusion

- **Design equations give can quickly produce values for macro model simulation**
- **Design equations predicts the required parameters with high accuracy (less than 7% error for SNDR and SNR)**

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References

1. T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway, and H.-S. Lee, “Comparator-based switched-capacitor circuits for scaled CMOS technologies,” in ISSCC Digest of Technical Papers, 2006, pp. 220–221.
2. C. Wulff and T. Ytterdal, “Design Of A 7-bit, 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In A 65nm CMOS Technology,” in Proc. NORCHIP 2007

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