Switched Capacitor Analog Modulo Integrator For Application In Open Loop Sigma-Delta Modulators

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***Abstract*— We introduce the switched capacitor analog modulo integrator, which to our knowledge is a new circuit. We introduce the amplitude modulated open loop $\Sigma\Delta$ modulator (OLSDM), which is an analog modulo integrator followed by a quantizer and a modulo differentiator. The mathematical equivalence between low pass $\Sigma\Delta$ modulators and OLSDM is explained. Behavioral simulations confirm the equivalence. The necessary circuit, a switched capacitor analog modulo integrator, is explained in detail. Behavioral level simulations in SPICE of the analog modulo integrator verify the function, and prove the concept of amplitude modulated OLSDM.**

***Index Terms*— $\Sigma\Delta$ Modulators, Switched Capacitor Circuits, Analog Modulo Integrator**

I. Introduction

$\Sigma\Delta$ modulators have become a natural choice for analog-to-digital conversion in applications with low to medium bandwidth and high resolution. The $\Sigma\Delta$ modulator shapes the spectral density of the quantization error of data converters. The quantization error, or as it is often called, quantization noise, is the error introduced by converting a continuous value signal into a discrete value signal. This error is often considered to have uniform spectral density, or in other words, be a white noise source. The conditions for considering quantization error as a white noise source was covered in [1].

The conventional low-pass $\Sigma\Delta$ modulator (L-SDM) in its simplest form consists of an integrator followed by a quantizer. The quantized signal is fed back to the input through a digital-to-analog converter (DAC) and subtracted from the input. The transfer function of the modulator is different for the input signal and the quantization noise. [1] The input signal will undergo an integration followed by a differentiation and have a transfer function of one. The quantization noise will be differentiated and thus high pass filtered.

In an ideal world, with no voltage swing limitations, an L-SDM system could be implemented by an integrator followed by a quantizer and a differentiator, but since supply voltage is limited in electronic circuits, and an integrator has infinite dc gain, it is difficult to implement. Somehow the output swing of the integrator has to be limited. Feedback is normally used to limit the output swing of the integrator.

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[1]This assumes a linear model of the quantizer, since the transfer function is only defined for a linear system

There are many different types of $\Sigma\Delta$ modulators. In this paper we discuss a small sub group that we denote Open Loop $\Sigma\Delta$ Modulators (OLSDM). We define an OLSDM as: Any $\Sigma\Delta$ modulator that does not have feedback of the quantized modulator output signal.

One of the first suggestion of an OLSDM can be found in [2]. Although there is no system implementation they explain a method that avoids the feedback DAC. More recently there have been others like the Frequency $\Sigma\Delta$ Modulator (FSDM) in [3] and [4].

In the FSDM a voltage to frequency converter, a voltage controlled oscillator (VCO), was used in place of the integrator, and it was shown in [3] that the pre-processing in FSDM is equivalent to modulo integration. The FSDM could be identified as a frequency modulated OLSDM.

In [5] they introduced the non-feedback $\Sigma\Delta$ digital-to-analog modulator where the integrator was implemented as a digital modulo integrator.

In the past the noise shaping of $\Sigma\Delta$ modulators has been combined with the high speed of pipelined ADCs. In [6] a second order five bit $\Sigma\Delta$ Modulator was cascaded with a 12 bit pipelined ADC. The output of the $\Sigma\Delta$ Modulator was combined with the output of the pipelined ADC to generate the digital output word. We wanted to investigate whether one could avoid any interaction, with the exception of the input and output signals, between the $\Sigma\Delta$ Modulator and the pipelined ADC in such a system. The question was; could one pre-process the input signal to implement the sigma, quantize and do post-processing to perform the delta, without interaction between the sigma and the delta. The block diagram of such a system is shown in Figure 1

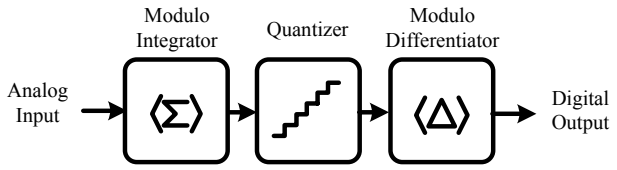

Fig. 1. First order OLSDM block diagram

We knew from [5] that the open loop $\Sigma\Delta$ modulator was possible when all blocks were digital, by using modulo integration, quantization and modulo differentiation. However, in an analog-to-digital OLSDM the modulo integration would have to occur in the analog domain. We were unable to find

any published circuit that matched our requirements for an analog modulo integrator. Accordingly, the switched capacitor analog modulo integrator was developed, which we present here. To our knowledge, this switched capacitor analog modulo integrator is a new circuit.

In Section II we elaborate on the mathematical equivalence between OLSDM and L-SDM, which is supported by behavioral simulations in Matlab in Section III. Quantizer nonlinearity and common errors are also discussed in Section III. In Section IV we introduce the analog switched capacitor modulo integrator. Behavioral level simulations with a SPICE macro model of the analog modulo integrator and the OLSDM are presented in Section V.

II. Open Loop ΣΔ Modulator

The most basic low pass OLSDM is an integrator, followed by a quantizer and a differentiator as illustrated by Figure 1. The input signal is integrated and afterwards differentiated, hence the output is equal to the input, assuming a linear system. The quantization error added by the quantizer is differentiated thus high pass filtered. To limit the swing in the analog domain we use a modulo operation at the output of the integrator. The inverse operation, which is also a modulo operation, is performed in the digital domain after the differentiator. A modulo operation is trivial to implement in the digital domain. The analog modulo operation is not trivial, and it has previously been implemented as a voltage to frequency converter in [3] and [4].

The equivalence of L-SDM and OLSDM was shown in [5]. Here we endeavor to explain the equivalence more intuitively.

The OLSDM has been modeled as a piecewise linear system. The modulo operation is a non-linear operation, but it can be seen as a piecewise linear system if we ignore the discontinuities when the modulo operation occurs. The quantizer has been modeled as a linear addition of noise. Figure 2 shows the complete modulator.

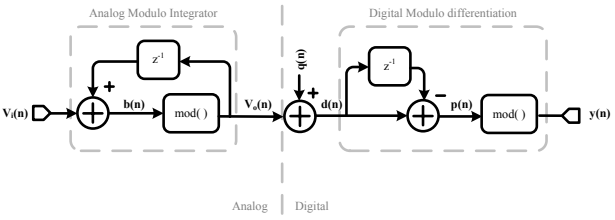

Fig. 2. Piecewise linear model of the OLSDM

The input signal to the modulator is $V_i(n)$, where n is the sample index. A signal with sample index n is the current sample while $n-1$ is the previous sample. The input is added to the previous output of the integrator, $V_o(n-1)$, resulting in $b(n)$. The signal $b(n)$ is subjected to modulo operation with $V_o(n)$ as a result. $d(n)$ is the sum of $V_o(n)$ and the quantization noise, $q(n)$. The differentiator output $p(n)$ is $d(n)$ minus the previous quantizer output $d(n-1)$. To get the output, $y(n)$, $p(n)$ is subjected to a modulo operation. In this system the second modulo operation cancels the first modulo operation and we have a system that is equivalent to an L-SDM. The equations in more detail follow.

We define the previous output from the integrator as

$$V_o(n-1) \in \langle -V_{ref}, V_{ref} \rangle \tag{1}$$

and the input signal as

$$V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \tag{2}$$

where V_{ref} is the reference voltage.

We know that after integration, but before the modulo operation, we get

$$b(n) = V_i(n) + V_o(n-1) \tag{3}$$

where $b(n)$ will be bounded by

$$b(n) \in \langle -V_r, V_r \rangle \tag{4}$$

where $V_r = 2V_{ref}$. The modulo operation is used to reduce the output swing to $V_o(n) \in \langle -V_{ref}, V_{ref} \rangle$. The modulo operation subtracts or adds V_r, depending on the value of the summation in (3). The next output from the integrator can be written as

$$V_o(n) = \begin{cases} b(n) + V_r & b(n) \in \langle -V_r, -V_{ref}] \\ b(n) & b(n) \in \langle -V_{ref}, V_{ref} \rangle \\ b(n) - V_r & b(n) \in [V_{ref}, V_r \rangle \end{cases} \tag{5}$$

Accordingly (5) is the equation for a modulo integrator. After quantization the input to differentiation will be

$$\begin{aligned} d(n) &= V_o(n) + q(n) \\ d(n-1) &= V_o(n-1) + q(n-1) \end{aligned} \tag{6}$$

where $q(n), q(n-1)$ are the quantization errors. The the output of the differentiator is

$$p(n) = d(n) - d(n-1) \tag{7}$$

If we in (7) insert for $d(n)$, $d(n-1)$, $V_o(n)$ and set $e(n) = q(n) - q(n-1)$ the expression becomes

$$p(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{8}$$

The bounds of $V_i(n)$ in (8) are derived from the possible input signal values for the modulator to reach the states in (8). Consider the first case where

$$p(n) = V_i(n) + V_r + e(n), V_i(n) \in \langle -V_{ref}, 0 \rangle \tag{9}$$

Here V_r has been added, thus

$$b(n) \in \langle -V_r, -V_{ref}] \tag{10}$$

from (5). For b(n) to have these bounds

$$V_i(n) \in \langle -V_{ref}, 0 \rangle \tag{11}$$

and

$$V_o(n-1) \in \langle -V_{ref}, 0 \rangle \tag{12}$$

This is sufficient to ensure the bounds of $p(n)$ in case 1 in (8) are

$$p(n) \in [V_{ref}, V_r \rangle$$

Thus when we apply another modulo operation we get

$$y(n) = \begin{cases} V_i(n) + V_r - V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \quad (13)$$

and for all cases in (13), $y(n) \in \langle -V_{ref}, V_{ref} \rangle$. Equation (13) can be expanded into

$$y(n) = V_i(n) + q(n) - q(n-1)$$

Which result in the well known equations

$$\frac{y(z)}{V_i(z)} = 1\,, \; \frac{y(z)}{q(z)} = 1 - z^{-1} \quad (14)$$

The transfer function from the input signal to the output is one, which is the same as for an L-SDM, although often the transfer function of an L-SDM from input to output contains a time delay, $y(z)/V_i(z) = z^{-1}$. The quantization error is differentiated, thus first order high pass filtered. This proof can be extended to higher order modulators.

III. Behavioral Simulations In Matlab

The behavioral simulations presented here are an implementation of the equations explained in the previous section. [2]

A. First And Second Order OLSDM

A first and second order OLSDM and an oversampled quantizer without noise shaping were modeled and simulated in Matlab. The oversampled quantizer without noise shaping was included to compare ideal results with the simulated results. All quantizers were implemented as 7 bit quantizers. An oversampling ratio (OSR) of 8 was chosen. An overview of the system can be seen in Figure 3.

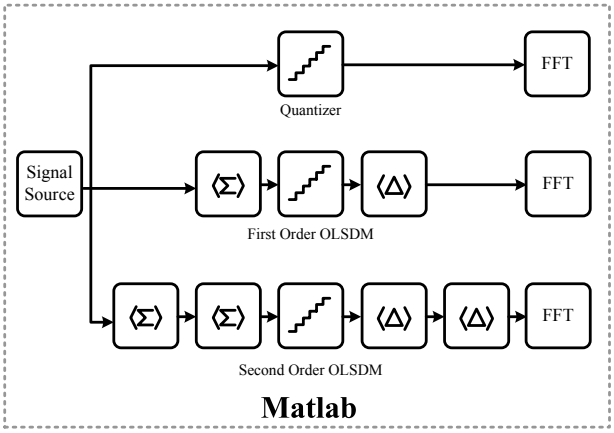

Fig. 3. Overview of behavioral level simulation system

The ideal signal to noise and distortion ratio (SNDR) for the different cases are shown in Table I. The ideal SNDR are based on equations from [7].

The equations for the OLSDM were implemented as specified in the previous section with one exception. We chose to implement the quantizer using unsigned integer outputs, the output ranging from 0-127. With this implementation $d(n)$ has a dc offset. The differentiator is a high pass filter and removes this dc offset. For the modulo operation to work, a dc offset was added after the differentiator to restore the correct common mode. In the second order OLSDM a dc offset was added after both differentiators.

[2]The Matlab code for the first and second order OLSDM can be downloaded from http://www.nextgenlab.net/olsdm

TABLE I
IDEAL SNDR FOR 7 BIT QUANTIZER, OSR=8

Noise Shaping	Improvement (dB)	Total (dB)
None	$10 \times \log(OSR)$	52.9
First order	$30 \times \log(OSR) - 5.17$	65.8
Second order	$50 \times \log(OSR) - 12.9$	76.1

The sampling frequency was chosen arbitrarily at 1MHz and the input signal was chosen according to the rules of coherent sampling [8]. In Matlab the sampling frequency is of no importance, we could just as well have used normalized frequencies. However, these simulations will be compared to SPICE simulations, and in SPICE the sampling frequency is of importance. The input frequency was $f_{in} = 6164.6Hz$ and 2^{15} samples of the output, $y(n)$, were calculated.

The input signal to the OLSDM must be limited, as specified in equation (2). It turns out that (2) is incorrect when we deal with a finite resolution quantizer, which we will discuss in the next section. For the remainder of this paper the input signal amplitude has been fixed at 0.9FSR, unless otherwise specified. As a consequence SNDR will be 0.91dB lower than ideal cases in Table I.

The outcome of simulations are summarized in Table II. Both the second order OLSDM and the first order OLSDM have approximately the same SNDR as the ideal modulators. When we remove the effects of reduced input amplitude we are left with an error of $+0.2dB$ for no noise shaping, $+0.01dB$ for first order OLSDM, and $-0.19dB$ for second order OLSDM, which is within the errors of the SNDR extraction.

The Fast Fourier Transform was used to extract the SNDR, the FFTs can be seen in Figure 4 and Figure 5. The light gray spectrum in the figures are the FFTs of the ideal 7 bit quantizer, which is the same for the two figures.

TABLE II
SNDR OF OLSDM MODULATORS WITH 2^{15} POINT FFT

Noise Shaping	Total (dB)	Difference from Ideal (dB)
None	52.2	-0.7
First order	64.9	-0.9
Second order	74.9	-1.1

B. Input Signal Amplitude Limitations

In the derivation of (2) we ignored quantization noise. But when we deal with a finite resolution quantizer, quantization noise cannot be ignored. With quantization noise (8) becomes

$$p(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) + e(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) + e(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) + e(n) \in \langle 0, V_{ref} \rangle \end{cases} \quad (15)$$

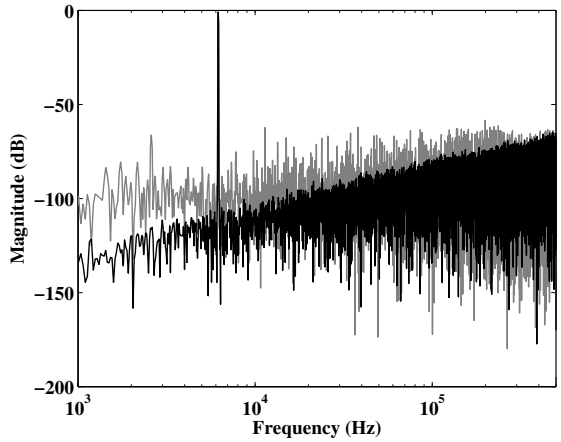

Fig. 4. 2^{15} point FFT of the first order OLSDM output

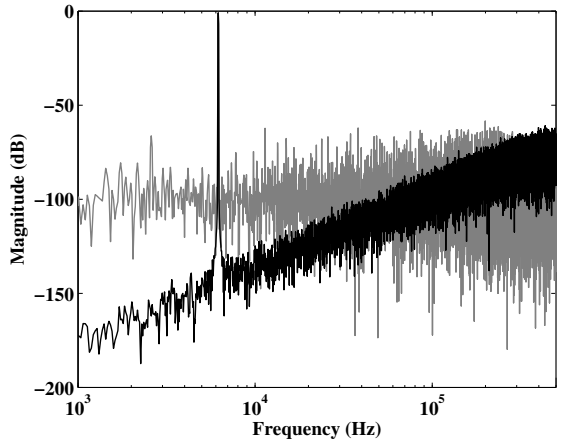

Fig. 5. 2^{15} point FFT of the second order OLSDM output

The boundaries of (15) now include the quantization noise. For example for case two, where

$$p(n) = V_i(n) + e(n)$$

no digital modulo should be performed. To make certain no digital modulo is performed

$$V_i(n) + e(n) \in \langle -V_{ref}, V_{ref} \rangle$$

accordingly

$$V_i(n) \in \langle -V_{ref} + |e(n)|, V_{ref} - |e(n)| \rangle \tag{16}$$

If the input amplitude is not limited as specified by (16), we get a condition we denote as *false modulo* errors. For example, assume that for case two in (15) we get

$$p(n) = V_i(n) + e(n) <= -V_{ref} \tag{17}$$

as a consequence

$$y(n) = V_i(n) + V_r + e(n) \tag{18}$$

here a modulo operation was carried out on $p(n)$ when it should not have been.

The limit in (16) indicate that low resolution quantizers may not be suited for this type of OLSDM.

These errors are easy to spot in the output of the OLSDM, shown in Figure 6. They cause large glitches which span the range of the output codes. To avoid these errors it is sufficient to limit the input signal. It should be noted that the presence of these errors completely removes the noise shaping of the OLSDM.

In the circuit implementation of the analog modulo integrator, described by equation (5), we use comparators to detect $b(n) \in \langle -V_r, -V_{ref}]$ and $b(n) \in [V_{ref}, V_r \rangle$. If we use the outputs from these comparators we can prevent the *false modulo* errors from occuring. In the first order OLSDM we know that a modulo should only be performed after differentiation when a modulo was performed in the analog modulo integrator. Consequently we can use the outputs of the comparators in the modulo integrator to control the modulo operation in the differentiator. This ensures that *false modulo* errors never occur. The solution comes at the cost of delay lines that must be added to synchronize the comparator outputs from the modulo integrators with the modulo differentiator. For the remainder of the paper we do not use this solution. In Section III-C we describe an error correction technique that corrects *false modulo* errors without using the comparator outputs.

Unrelated to these errors it was shown in [9] that for digital-to-analog OLSDM $N+1$ quantizer bits are normally needed, where N is the OLSDM order. Thus for a second order OLSDM we would need a 3 bit quantizer. We expect the same to be true for analog-to-digital OLSDM.

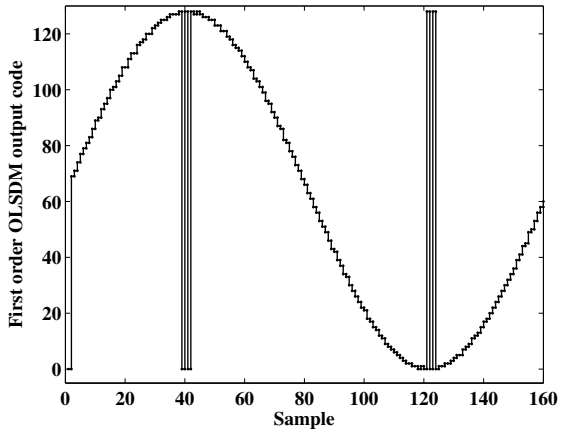

Fig. 6. The output of the first order OLSDM in the presence of *false modulo* errors

C. Quantizer Linearity And Correction Of False Modulo Errors

An important issue of the amplitude modulated OLSDM is how the linearity of the quantizer affects the system. The step sizes in the quantizer were made dependent on the input signal, thus introducing a non-linearity. By changing the dependence on the input signal we control the linearity of the quantizer. In this example an 7 bit quantizer with a

maximum of 6.8 bit linearity was used as the quantizer in the second order OLSDM. The results are presented for two different input amplitudes, $0.8FSR$ and $0.9FSR$. Figure 7 shows the linearity of the OLSDM as a function of quantizer linearity. As expected, the linearity of the OLSDM does depend on the linearity of the quantizer. For each bit of reduction in the linearity of the quantizer the second order OLSDM looses half a bit of linearity. The slope is constant until a threshold is reached, the threshold marks the onset of *false modulo* errors. Below this threshold the SNDR of the OLSDM degrades rapidly. The threshold is highly dependent on the input amplitude and is on the order of (16). Such a sharp decrease in SNDR at a particular input signal amplitude is undesirable, and it would be advantageous to correct for the cause of the sharp degradation, the *false modulo* errors. As mentioned we can use the comparator output from the analog modulo integrators to control modulo differentiation, which will remove the *false modulo* errors. However, there is an alternate solution.

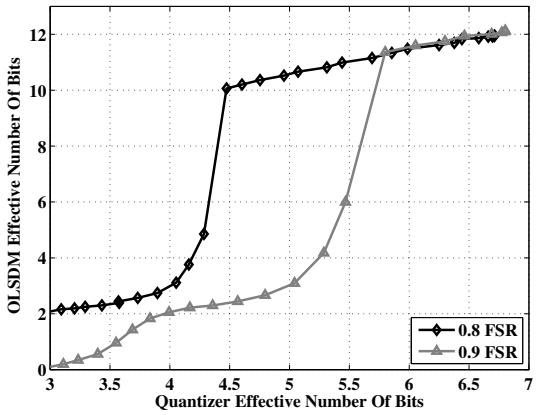

Fig. 7. Linearity of second order OLSDM as a function of quantizer linearity

The *false modulo* errors have a large amplitude and high frequency, as seen in Figure 6. They span the range of the output codes in two samples, and thus have a frequency close to the Nyquist frequency. If we take advantage of the fact that the input signal is, by choice, at least eight times lower than the Nyquist frequency, since we chose an OSR of eight, we can reduce the errors. There is a maximum difference between two adjacent output codes, which depend on the input signal. We assume a sinusoidal input at one-eight of the Nyquist frequency. A sinusoid has a maximum slope at the zero crossing which is approximately given by

$$Slope \approx A\pi/OSR \tag{19}$$

, where A is the amplitude. In (19) we have used the well known assumption that $\sin x \approx x$ if x is small and that $OSR = f_s/2f_{in}$. With an OSR of eight $Slope \approx 0.39$ at zero crossing, which is approximately one fifth of the FSR.

We assume that any change in the output of more than $0.6FSR$ between two consecutive samples is due to a *false modulo* error. If two consecutive samples of the OLSDM output has a difference of more than 0.6FSR we undo the modulo operation. The result of this simple correction can be seen in Figure 8. The error correction compensates for the dependence on input signal amplitude and the onset of *false modulo* errors. It should be noted that this error correction technique now allows the input signal amplitude to be FSR.

In this error correction technique we have made an assumption on the properties of the output signal of the modulator. In this assumption we must be cautious of the quantization noise. If we use a low resolution quantizer the quantization noise power at higher frequencies can be significant, and output codes which span the range of output codes in two samples are certainly possible. Having said that, with higher resolution quantizer and low order noise shaping the quantizer noise power is not significant enough to influence the error correction.

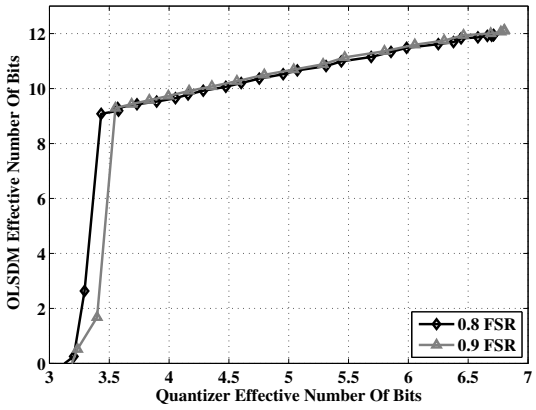

Fig. 8. Linearity of second order OLSDM as a function of quantizer linearity with error correction enabled

The circuit implementation of an amplitude modulated OLSDM requires an analog modulo integrator. The next section explains how such a function can be implemented by a switched-capacitor circuit.

IV. The Analog Modulo Integrator

A requirement set on the analog modulo integrator was that it should use maximum swing available, for example 0.8V peak-to-peak with 1.2V supply. It should also be a discrete time system and it should be amplitude modulated and not frequency modulated as was used in [3] and [4]. The discrete time equation for a analog modulo integrator was shown in (5).

Using pseudo code the modulo integrator can be described as

1) Add the previous output to the current input
2) If the new output is equal to or exceeds the reference voltages
3) Subtract/Add the range of the integrator, V_r
4) Set the current output to the remainder

A modulo operation is trivial to implement in the digital domain, but it may not be obvious how it should be implemented in the analog domain. Adding two voltages in the analog domain is conceptually trivial. Whether a voltage exceeds a

reference can be detected using a comparator. Subtraction in the analog domain is also trivial, but keeping the remainder presents a challenge.

Assume that the reference voltages are symmetric around the common mode, such that $|V_{ref}| = |-V_{ref}|$ and $|V_{ref}| + |-V_{ref}| = V_r$. The maximum internal voltage in the modulo integrator would be less than $V_{ref} + V_{ref} = V_r$ or more than $-V_{ref} + -V_{ref} = -V_r$. So the output after summation, but before modulo operation, will be bounded by

$$-V_r < b(n) < V_r \tag{20}$$

In a circuit where the analog value is represented by voltages the swing would have to be $2V_r$ to accurately represent all analog values. Since our input signal has a range of V_r we would waste an extra range of V_r just to represent intermittent values in the integrator. It would be better if we could set the voltage swing of the circuit to V_r, which is equal to the maximum input swing. But in a circuit where the analog values are represented with voltages this is difficult.

A. A Solution Based On Switched Capacitors

Switched-Capacitor (SC) circuits are prevalent in many analog integrated circuits. In discrete time $\Sigma\Delta$ modulators it is common to implement the integrator with a switched-capacitor circuit. It turns out that with small modifications a switched-capacitor integrator can be converted to an analog modulo integrator.

In switched-capacitor circuits the analog values are represented by voltages across charged capacitors. A conventional switched-capacitor integrator, shown in Figure 9, adds the previous output and current input.

This simple integrator has two phases, sample ($\phi 1$) and charge transfer ($\phi 2$). Assume the charge stored on C_2 is zero ($Q_2 = 0$). In the sample phase we charge C_1 to the input voltage, thereby placing a charge of $Q_1 = V_i C_1$ on the capacitor. During charge transfer the charge of C_1 is transferred to C_2 by forcing the voltage V_g to be equal to ground using an operational amplifier. The voltage across C_1 is then zero and there is no charge stored across it, all charge is across C_2. This causes the output voltage to be $V_o(n) = Q_1/C_2$. If the input value is kept constant, the next output value, after a clock cycle, will be $V_o(n+1) = 2Q_1/C_2$.

In the charge transfer phase V_g is a high impedance node, thus the total charge, Q_{tot}, given by $Q_{tot} = Q_1 + Q_2$, does not change. Q_{tot} is independent of the voltages at V_g and V_o. Thus we can argue that the ideal output value, $V_{o-ideal} = Q_{tot}/C_2$ is only dependent on the total charge across the capacitors. By ideal output voltage $V_{o-ideal}$ we mean the output voltage V_o if V_g was forced to ground.

A real world operational amplifier will normally have a maximum output signal swing. For example, if we exceed this signal swing the gain in the operational amplifier goes down, and it is unable to force virtual ground. In this case V_o saturates, it cannot go any higher, hence $V_o < V_{o-ideal}$. This saturation voltage we define as $V_{sat} > V_{ref}$.

Assume that the operational amplifier saturates in $\phi 2$, hence $V_o = V_{sat} > V_{ref}$. If we can detect this condition, $V_o > V_{ref}$, we can subtract a charge from V_g that represents V_r ($V_r = 2V_{ref}$ as defined in Section II), thus perform a modulo operation. We would now have

$$V_{o-ideal} = (Q_{tot} - Q_{V_r})/C_2 < V_{ref} < V_{sat}$$

as a consequence the operational amplifier will be able to force virtual ground.

One of the differences between the switched capacitor analog modulo integrator and the conventional integrator is that the latter has three clock phases. The first two have the same function as in the conventional integrator, sample and charge transfer. The third clock phase is added to detect if $V_o > V_{ref}$ (and the opposite, $V_o < -V_{ref}$) in phase two. If it does exceed, a charged capacitor is connected to the charge transfer node of the integrator, node V_g in Figure 9. This subtracts or adds the charge which represent V_r. This will change the charge transfer equation, and as we shall see, implement a modulo operation.

Provided that the input signal limited as specified by (16), the subtracted/added charge will ensure that

$$-V_{ref} < V_o < V_{ref} \tag{21}$$

The circuit needed to implement a modulo integrator is shown in Figure 10. It is connected to the integrator in node V_g and V_o. The complete circuit has, as mentioned, three clock phases; $\phi 1$, $\phi 2$ and $\phi 3$. The timing diagram is shown in Figure 11, where T denotes the period and $1/3, 2/3$ denotes the fractional time steps.

Consider the integrator in Figure 9. During clock phase $\phi 1$ the input signal is sampled across capacitor C1. In clock phase $\phi 2$, before $\phi 3$, the charge from C1 is transferred to C2. The charge transfer equation will be

$$C_2 V_o(n - T/3) = C_2 V_o(n - T) + C_1 V_i(n - 2T/3) \tag{22}$$

In this equation, $V_o(n-T/3)$, is equivalent to $b(n)$ from equation (3) and will have the same bounds, assuming $C_1 = C_2$. For the output, $V_o(n)$, to stay within the reference voltages, V_r has to be added or subtracted as in equation (5).

Figure 12 shows the states of Figure 10 in more detail. During $\phi 1$, Figure 12 a) , the capacitor C_3 is charged to $V_r = V_{ref} - -V_{ref}$. At the start of $\phi 3$ the latched comparators ($X2$ and $X3$ in Figure 10) determine whether the output voltage exceeds the reference. Figure 12 b) shows the connections if the output voltage, $V_o(n - T/3)$, is higher than V_{ref}. Here a charge of $Q_3 = C_3 V_r$ is transferred to the node V_g in the

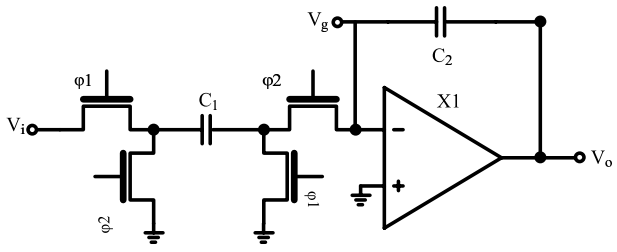

Fig. 9. Conventional switched capacitor integrator

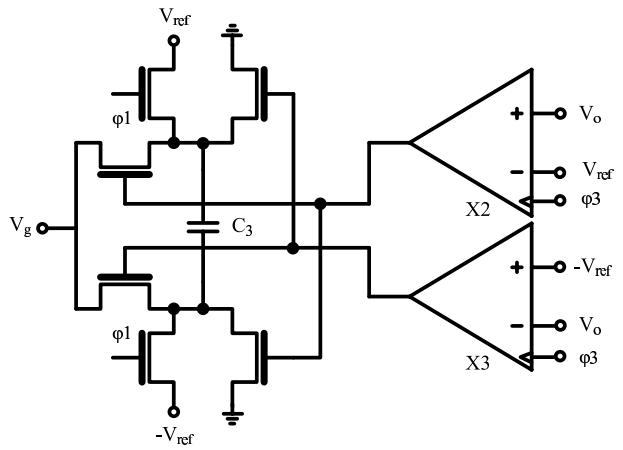

Fig. 10. Modulo circuit

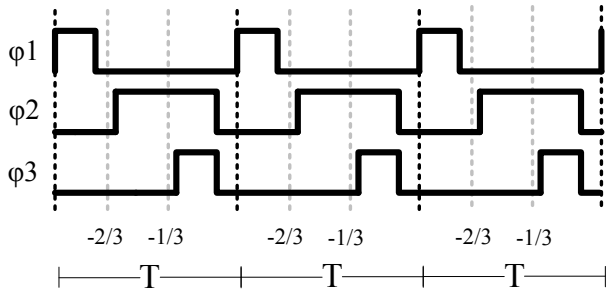

Fig. 11. Timing diagram for the modulo integrator

integrator. This will change the charge transfer equation into

$$C_2V_o(n) = C_2V_o(n-T) + C_1V_i(n-2T/3) - C_3V_r \quad (23)$$

For $V_o(n-T/3)$ lower than $-V_{ref}$, Figure 12 c) , the polarity of the charge is reversed and the charge transfer function is

$$C_2V_o(n) = C_2V_o(n-T) + C_1V_i(n-2T/3) + C_3V_r \quad (24)$$

And if $-V_{ref} < V_o(n-T/3) < V_{ref}$ the capacitor C_3 is not connected to V_g and the charge transfer function (22) remains unchanged as shown in Figure 12 d). Notice that the outputs from the comparators can never be high at the same time.

Combining the three equations, (22), (23) and (24) with $C_1 = C_2 = C_3$ and ignoring the fractional time-steps ($n-T/3$ and $n-2T/3$) the result is (5).

The analog modulo integrator presented here resemble a first-order low pass 1.5 bit $\Sigma\Delta$ Modulator. If one plots the spectrum of the combined comparator outputs it is a quantized first order noise shaped version of the input. What makes an analog modulo integrator different from a first order low pass $\Sigma\Delta$ Modulator is

- The quantizer levels are set at $\pm V_{ref}$, and not evenly distributed between $\pm V_{ref}$.
- The three phase clock implements a form of zero time quantizer feedback, if V_o is higher than V_{ref} V_r is immediately subtracted before the next output of the integrator.
- The comparator outputs are not necessary to reverse the effect of the modulo operation in the digital domain.

V. Behavioral Level Verification Of The SC OLSDM

We implemented a macro model description of the SC analog modulo integrator described in the previous section.[3] A single pole operational amplifier macro model with a dc gain of 74dB and a voltage limiter was used to model the operational amplifier. The comparators were modeled as latched comparators. Ideal switches with an on resistance of 200 Ohms were used and the capacitors C1-C3 were 5pF. The reference voltages were $V_{ref} = 1V$ and $-V_{ref} = -1V$. The switch resistance, capacitance and references were chosen arbitrarily. The output of the operational amplifier was limited to $\pm 1.4V$. This ensures that for some values of the input the integrator will saturate during $\phi 2$. The input frequency, sampling frequency and the number of samples was the same as for the Matlab simulation. An overview of the system can be seen in Figure 13.

Only the analog modulo integrator was implemented in SPICE. Its output was extracted and post-processed in Matlab. The code for the differentiator and the quantizer were the same as in the behavioral simulations.

In Figure 14 the input signal (dark gray) and the output signal (light gray) of the first order SC modulo integrator is shown for the first 150 samples. The sinusoidal input had an amplitude of $0.9V$. The output, V_o, has been sampled at the end of $\phi 3$ and it can be seen how it never exceeds the references at V_{ref} and $-V_{ref}$.

A transient simulation was performed. The results are summarized in Table III. If we remove the effect of reduced input signal amplitude the errors are $-0.2dB$ for first order OLSDM and $-2.1dB$ for second order OLSDM. The error for first order OLSDM is within the error of the SNDR extraction. The error for the second order OLSDM it is to large to be caused by deviations due to SNDR extraction. This extra loss of $-2.1dB$ was mainly due to non-linearity of the voltage limiter used in the simulation. When the voltage limiter is removed the error for second order OLSDM is reduced to $-0.79dB$. The remaining difference is mostly due to finite gain in the operational amplifier. The FFTs of the first and second order OLSDM are shown in Figure 15 and Figure 16, the ideal quantizer in light gray and the OLSDM output in dark gray.

TABLE III
SNDR of OLSDM modulators in SPICE

Noise Shaping	Total (dB)	Difference from Ideal (dB)
First order	64.7	-1.1
Second order	73.1	-3

VI. Future Work

There are no integrated circuit implementations of an amplitude modulated OLSDM as of yet. An integrated circuit implementation would be the next step. It is needed to check whether the amplitude modulated OLSDM has a place in the

[3]The SPICE macro model of the switched capacitor analog modulo integrator can be downloaded from http://www.nextgenlab.net/olsdm

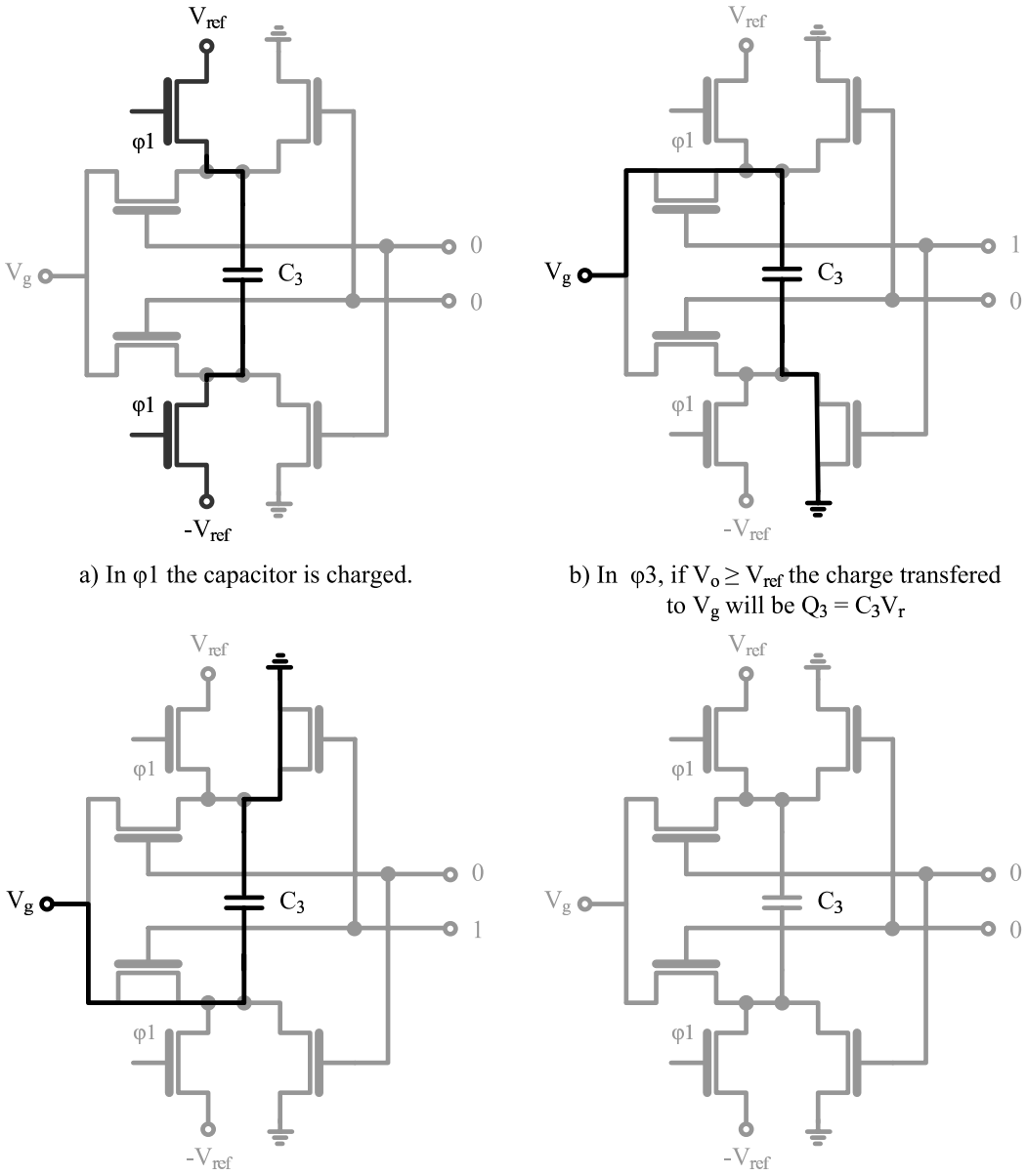

Fig. 12. The states of the modulo circuit in Figure 10

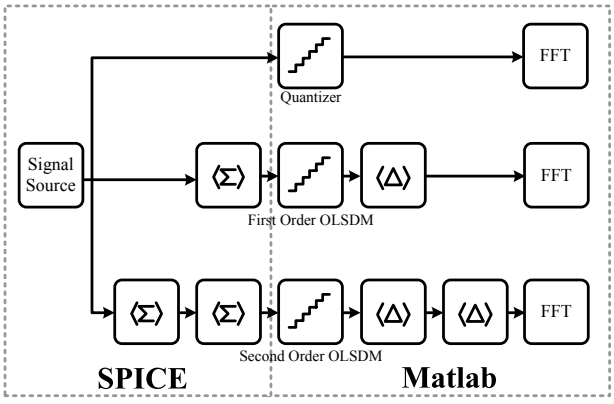

Fig. 13. Overview of circuit simulation with macro models

family of analog-to-digital converters, or whether it is just of academic interest. There are many questions to be answered and some questions that have not yet been asked. The switched capacitor analog modulo integrator is, to our knowledge, new circuit, and it may find applications outside the realm of OLSDM.

VII. Conclusion

We introduced the switched capacitor analog modulo integrator, which to our knowledge is a new circuit. We introduced the amplitude modulated open loop ΣΔ modulator (OLSDM), which is an analog modulo integrator followed by a quantizer and a modulo differentiator. The mathematical equivalence between low pass ΣΔ modulators and OLSDM was explained.

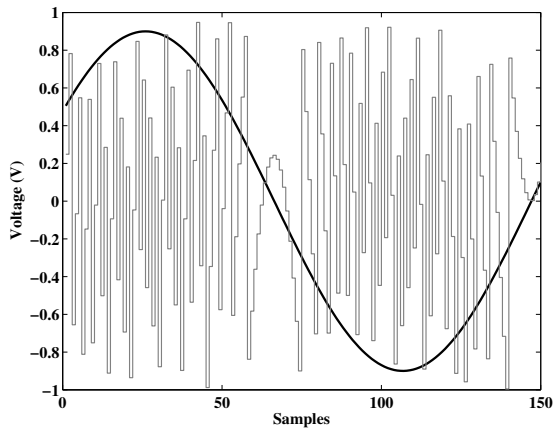

Fig. 14. Input vs output for the modulo integrator. Input is a sine with an amplitude of 0.9 V

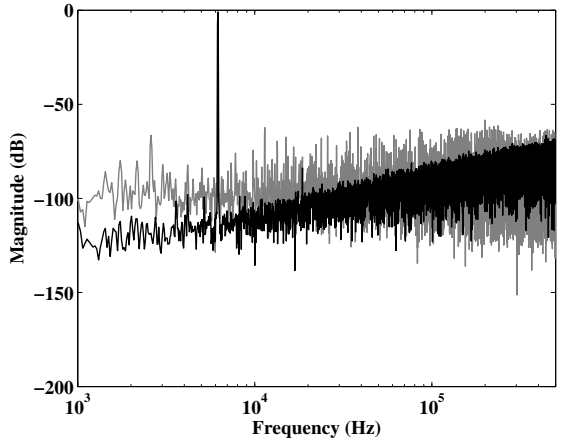

Fig. 15. FFT of output from first order OLSDM simulation in SPICE.

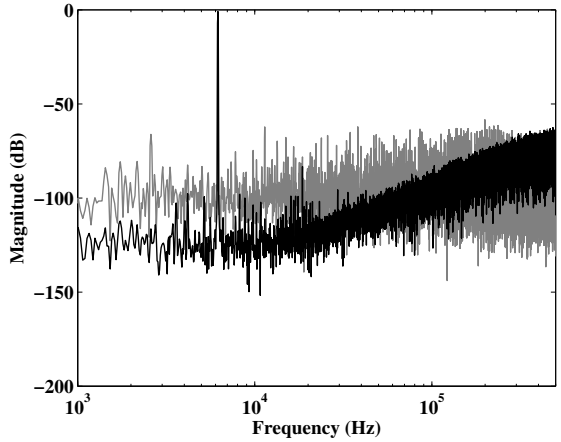

Fig. 16. FFT of output from second order OLSDM simulation in SPICE.

Behavioral simulations confirmed the equivalence. The necessary circuit, a switched capacitor analog modulo integrator, was explained in detail. Behavioral level simulations in SPICE of the analog modulo integrator verified the function, and proved the concept of amplitude modulated OLSDM.

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Financial support from the Norwegian Research Council through the project Smart Microsystems for Diagnostic Imaging in Medicine (project number 159559/130) and the project ASICs for Microsystems (project number 133952/420) is gratefully acknowledged.

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