Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

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***Abstract*— A switched-capacitor analog modulo integrator is presented. This analog modulo integrator makes it possible to design an Open-Loop Sigma-Delta Modulator (OLSDM). The theory of OLSDM and analog modulo integration is explained and verified through simulation.**

I. Introduction

Sigma-Delta modulators have become a natural choice for analog to digital conversion in applications with low to medium bandwidth and high resolution. They are used in applications from high resolution instrumentation systems to ADSL communication systems. The purpose of the Sigma-Delta modulator is to shape the quantization error such that the spectral density of the quantization noise is non-uniform, the quantization error can for example be high-pass or bandpass filtered.

The Low-pass Conventional Sigma-Delta Modulator (LC-SDM) in its simplest form consists of an integrator followed by a quantizer. The quantized signal is fed back to the input through a digital-to-analog converter and subtracted from the input. The transfer function of the modulator will be different for the input signal and the quantization error of the quantizer. The input signal will normally undergo an integration followed by a differentiation and have a transfer function close to one. The quantization error will be differentiated and thus high pass filtered.

Ideally this system could be implemented by an integrator followed by a quantizer and a differentiator. However, an ideal integrator has infinite DC gain, and with limited input swing in analog electronic circuits, an ideal integrator is not possible to implement. This is the reason why feedback is used, the feedback serves to limit the signal swing.

Another approach to Sigma-Delta modulators is the Frequency Sigma-Delta Modulator (FSDM) [1]. Here an amplitude to frequency modulator was used instead of an integrator, similar to what was suggested in [2]. It was shown in [1] that the preprocessing in FSDM is equivalent to modulo integration.

In [3] they introduced the non-feedback Sigma-Delta digital-to-analog converter. Here the integrator was implemented as a digital modulo integrator.

This paper introduces an analog modulo integrator for use in OLSDM. The outline of this paper is as follows. Section II explains that OLSDM are mathematically equivalent to LC-SDM. In Section III the analog switched-capacitor modulo integrator is presented, to our knowledge, it is the first of its kind. System simulations in Section IV of the OLSDM verify the theory.

II. Open Loop Sigma-Delta Modulator

A. Proof of Equivalence

The equivalence of LC-SDM and OLSDM was shown in [3]. We endeavor to explain the equivalence in a more intuitive way.

The OLSDM has been modeled as a quasi-linear system. Quasi-linear since the modulo integration and modulo differentiation are stepwise linear. The quantizer has been modeled as a linear addition of noise. Figure 1 shows the complete modulator. It should be noted that this system is similar to the system presented in Figure 1 in [2], but they used a form of FM modulation to implement the modulo integration.

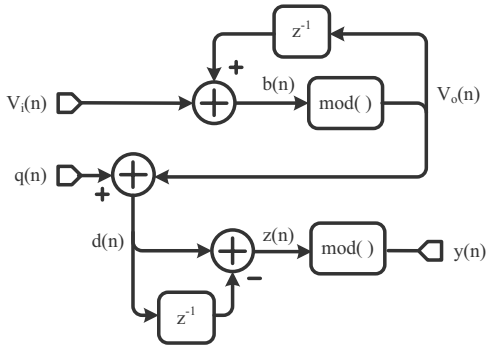

Fig. 1. Quasi-linear model of OLSDM

We define the previous output from the integrator as

$$V_o(n-1) \in \langle -V_{ref}, V_{ref} \rangle \tag{1}$$

and the input signal as

$$V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \tag{2}$$

where V_{ref} is the reference voltage.

We know that after integration, but before the modulo operation, we get

$$b(n) = V_i(n) + V_o(n-1) \tag{3}$$

where $b(n)$ will be bounded by

$$b(n) \in \langle -V_r, V_r \rangle \tag{4}$$

where $V_r = 2V_{ref}$. The modulo operation is used to reduce the output swing to $V_o(n) \in \langle -V_{ref}, V_{ref} \rangle$. The modulo operation

subtracts or adds V_r, depending on the value of the summation in (3). The next output from the integrator can be written as

$$V_o(n) = \begin{cases} b(n) + V_r & b(n) \in \langle -V_r, -V_{ref}] \\ b(n) & b(n) \in \langle -V_{ref}, V_{ref} \rangle \\ b(n) - V_r & b(n) \in [V_{ref}, V_r \rangle \end{cases} \quad (5)$$

After quantization the input to differentiation will be

$$\begin{aligned} d(n) &= V_o(n) + q(n) \\ d(n-1) &= V_o(n-1) + q(n-1) \end{aligned} \quad (6)$$

where $q(n), q(n-1)$ are the quantization errors. The the output of the differentiator is

$$z(n) = d(n) - d(n-1) \quad (7)$$

If we in (7) insert for $d(n)$, $d(n-1)$, $V_o(n)$ and set $e(n) = q(n) - q(n-1)$ the expression becomes

$$z(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \quad (8)$$

Thus, the output of the modulator is

$$y(n) = \begin{cases} V_i(n) + V_r - V_r + e(n) \\ V_i(n) + e(n) \\ V_i(n) - V_r + V_r + e(n) \end{cases} \quad (9)$$

and for all cases in (9), $y(n) \in \langle -V_{ref}, V_{ref} \rangle$, if we ignore the quantization error. This gives us the well known equations

$$\frac{y(z)}{V_i(z)} = 1 \, , \, \frac{y(z)}{q(z)} = 1 - z^{-1} \quad (10)$$

The transfer function from the input signal to the output is one, which is the same as for a LC-SDM (often the transfer function of a LC-SDM from input to output contains a time delay, $y(z)/V_i(z) = z^{-1}$). The quantization error is differentiated, thus first order high pass filtered. This proof can be extended to higher order modulators.

III. The Analog Modulo Integrator

As shown, the modulo integrator is an integrator that resets when the output increases or decreases beyond a reference voltage. It keeps the remainder that exceeds the reference voltage. A requirement set on the analog modulo integrator is that it should use maximum swing available, for example 0.8V peak-to-peak with 1.2V supply. It should also be a discrete time system. The discrete time equation for a modulo integrator was shown in (5).

Using pseudo code the modulo integrator can be described as

1) Add the previous output to the current input
2) If the new output exceeds the reference voltages
3) Subtract/Add the range of the integrator, V_r
4) Set the current output to the remainder

This is trivial to implement in the digital domain, but it may not be obvious how it should be implemented in the analog domain. Adding two voltages in the analog domain is conceptually trivial. Whether a voltage exceeds a reference can be detected using a comparator. Subtraction in the analog domain is also trivial, but keeping the remainder presents a challenge.

Assume that the reference voltages are symmetric around the common mode, such that $|V_{ref}| = |-V_{ref}|$ and $|V_{ref}| + |-V_{ref}| = V_r$. The maximum voltage would be less than $V_{ref} + V_{ref} = V_r$ or more than $-V_{ref} + -V_{ref} = -V_r$. So the output after summation, but before modulo operation, will be bounded by

$$-V_r < b(n) < V_r \quad (11)$$

In a circuit where the analog value is represented by voltages the swing would have to be $2V_r$ to accuratly represent all analog values. Since our input signal has a range of V_r we would waste an extra range of V_r just to represent intermittent values in the integrator. It would be best if we could set the voltage swing of the circuit to V_r, which is equal to the maximum input swing. But in a circuit where the analog values are represented with voltages this is difficult.

A. A Solution Based on Switched Capacitors

Switched-Capacitor (SC) circuits are prevalent in many analog integrated circuits. In discrete time Sigma-Delta modulators it is common to implement the integrator with a switched-capacitor circuit. It turns out that with small modifications a switched-capacitor integrator can be converted to an analog modulo integrator.

Realizing that in a switched capacitor integrator the analog value is stored as charge and not as voltages is the key to understanding how a modulo integrator can be implemented. A conventional switched-capacitor integrator, shown in Figure 2, adds the previous output and current input. When the integrator has settled, or failed to settle due to saturation of the opamp, it can be detected whether the output voltage exceeds the reference voltage. If it does exceed, a charged capacitor is connected to the charge transfer node of the integrator, node V_g in Figure 2. This subtracts/adds the charge which represent V_r. Provided that the input signal to the integrator never exceeds positive or negative reference, the subtracted/added charge will bring the integrator back within bounds. Since the analog information is stored in charge, the remainder is conserved.

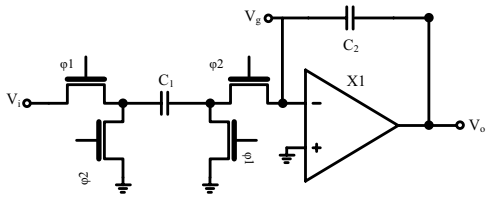

Fig. 2. Conventional Switched-Capacitor Integrator

B. Equations of the SC Modulo Integrator

The circuit needed to implement a modulo integrator is shown in Figure 3. It is connected to integrator in node V_g

and V_o. The complete circuit has three clock phases; $\phi 1$, $\phi 2$ and $\phi 3$. The timing diagram is shown in Figure 4, where T denotes the period.

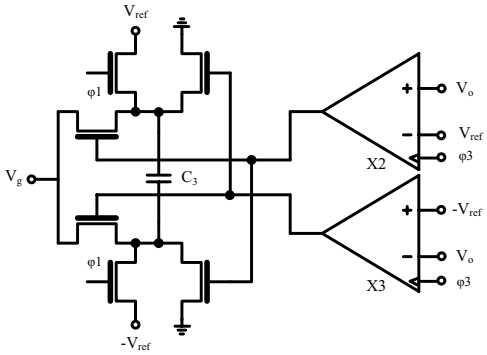

Fig. 3. Modulo circuit

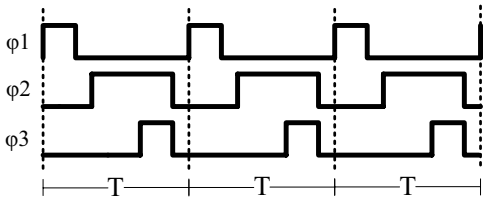

Fig. 4. Timing diagram for the modulo integrator

Consider the integrator in Figure 2, during clock phase $\phi 1$ the input signal is sampled across capacitor C1. In clock phase $\phi 2$, before $\phi 3$, the charge from C1 is transfered to C2. The charge transfer equation will be

$$C_2V_o(n-T/3) = C_2V_o(n-T) + C_1V_i(n-2T/3) \quad (12)$$

In this equation the output, $V_o(n-T/3)$, is equivalent to $b(n)$ from (3) and will have the same bounds, assuming $C_1 = C_2$. To make sure that the final output, $V_o(n)$, stays within the reference voltages, V_r has to be added or subtracted as in (5).

To perform the addition/subtraction the circuit in Figure 3 is used. The different states of this circuit are shown in Figure 5. During $\phi 1$, Figure 5 a), the capacitor C_3 is charged to $V_r = V_{ref} - -V_{ref}$. During $\phi 3$ the latched comparators ($X2$ and $X3$ in Figure 3) determine whether the output voltage exceeds the reference. Figure 5 b) shows the connections if the output voltage, $V_o(n-T/3)$, is higher than V_{ref}. Here a charge of $Q_3 = C_3V_r$ is transfered to the node V_g in the integrator. This will change the charge transfer equation into

$$C_2V_o(n) = C_2V_o(n-T) + C_1V_i(n-2T/3) - C_3V_r \quad (13)$$

For $V_o(n-T/3)$ lower than $-V_{ref}$, Figure 5 c), the polarity of the charge is reversed and the charge transfer function is

$$C_2V_o(n) = C_2V_o(n-T) + C_1V_i(n-2T/3) + C_3V_r \quad (14)$$

And if $-V_{ref} < V_o(n-T/3) < V_{ref}$ the capacitor C_3 is not connected to V_g and the charge transfer function (12) remains unchanged. Notice that the outputs from the comparators can never be high at the same time, because $V_o(n-T/3)$ cannot be higher than V_{ref} and lower than $-V_{ref}$ at the same time.

Combining the three equations, (12), (13) and (14) with $C_1 = C_2 = C_3$ and ignoring the frational timesteps ($n-T/3$ and $n-2T/3$) the result is (5).

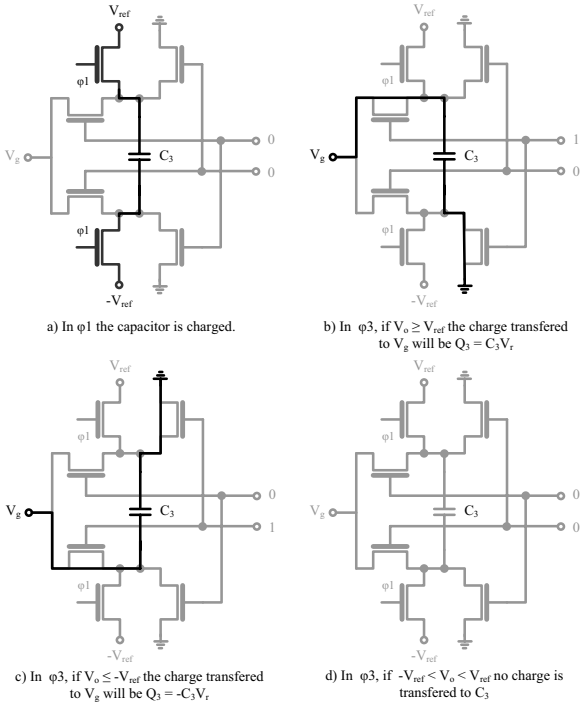

Fig. 5. The different permutations of the modulo circuit

C. Simulation of the SC modulo integrator

Simulation of the SC modulo integrator have been performed in AimSPICE [4] using ideal models for comparators, switches and operational amplifier.

In Figure 6 a DC input signal $V_i = 0.3V$ was used, the reference voltages were set to 1V. At around 5μ the integrator resets, here the output value would be $1.2V$ if it was not reset, and we can clearly see that the remainder is conserved

$$-1V + 0.2V = -0.8V \quad (15)$$

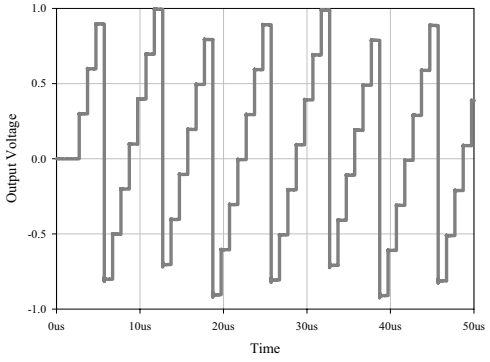

Fig. 6. Input vs output for the modulo integrator with constant input $V_i = 0.3V$

In Figure 7 the input and output for a sinusoidal input to the analog modulo integrator is shown. The reference voltage, V_{ref}, was set to 1V. The sinusoidal input had an amplitude of $0.99V$. The output has been sampled at the end of $\phi 3$ and it can be seen how it never exceeds the references at V_{ref} and $-V_{ref}$.

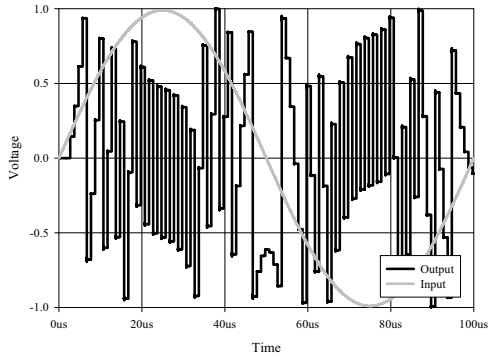

Fig. 7. Input vs output for the modulo integrator. Input is a sine with an amplitude of 0.99 V

IV. Simulation of OLSDM Modulator

The OLSDM was modeled in SystemDotNet [5], which is a mixed-signal discrete-time event driven simulator. A third order OLSDM with 8 bit quantizer was modeled. The spectral density plot can be seen in Figure 8. From the plot we can clearly see that we have third order high-pass filtering of the quantization noise since the slope of the noise floor is 60dB per decade. The dark-gray plot is an oversampled quantizer without noise shaping, shown for comparison. With an oversampling ratio of eight we get an ENOB (Effective Number Of Bits) of 15 bits. With just oversampling, no noise shaping, we get an ENOB of 9.5 bits.

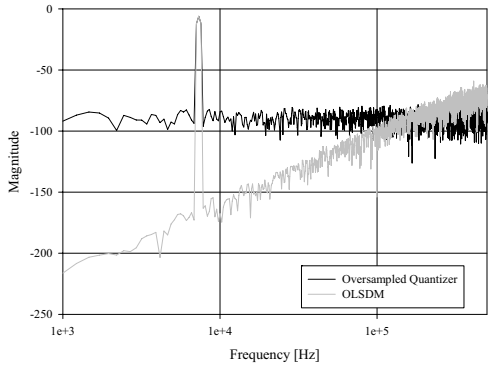

Fig. 8. Simulation of third order, 8 bit OLSDM. Input signal amplitude is 0.5 and sampling frequency is 1MHz. Also shown is the output from a oversampled quantizer without noise shaping

The analog modulo integrator can be compared to a first order, 1.5 bit LC-SDM. In Figure 9 we have plotted the output from the OLSDM and the combined outputs from the comparators in the analog modulo integrator (outputs of X2 and X3 in Figure 3). We can clearly see that the combined output of the comparators is a first order noise shaped version of the input signal. One could summize that the analog modulo integrator is just a 1.5 bit LC-SDM, but that would be inaccurate. If we assume the input signal is bounded by (2), the analog modulo integrator output will never exceed $-V_{ref}$ or V_{ref}, altough the output during $\phi 2$ might saturate. For the LC-SDM the input signal swing is normally reduced such that the output of the integrator does not saturate.

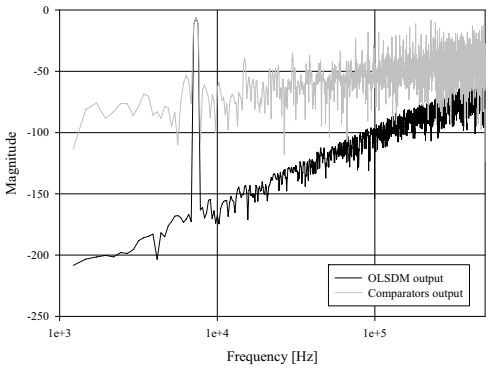

Fig. 9. The combined output of the comparators and the output of the OLSDM

V. Future Work

The OLSDM architecture with analog modulo integrator is, to our knowledge, a new architecture. Thus there are many questions to be answered and some questions that have not yet been asked. Research is currently being performed on the effects of mismatch, finite opamp gain, non-linearity of quantizer, finite number of bits in quantizer, and effects of parasitics. We hope to have an answer to some of these questions in the near future.

VI. Conclusion

A switched-capacitor analog modulo integrator was presented. This analog modulo integrator made it possible to design an Open-Loop Sigma-Delta Modulator (OLSDM). The theory of OLSDM and analog modulo integration was explained and verified through simulation.

Acknowledgments

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