High Speed, High Gain OTA in a Digital 90nm CMOS Technology

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***Abstract*— The design of a high-speed, high gain OTA in a digital $90nm$ CMOS technology is presented. The OTA uses the gain enhancement technique outlined in [1] to increase the DC gain. The amplifier is fully differential an utilizes fully differential gain enhancement OTAs. The frequency response shows that $70dB$ DC gain and a unity gain frequency of $2.5GHz$ is achieved. The OTA draws $20mA$ from a $1.2V$ power supply.**

I. Introduction

High performance A/D converters and switched capacitor filters require OTAs that have both high DC gain and a high unity gain frequency. The advent of deep sub-micron technologies enable increasingly high speed circuits, but makes designing high DC gain OTAs more difficult [2]. The OTA presented here is intended for a 10-bit pipeline ADC, thus making the required DC gain $60dB$ at full swing. By using a single stage cascode architecture with gain enhancement, the OTA can achieve both the speed and the gain requirements [1]. The cost is an increase in size and power consumption.

A cascode gain stage utilizes cascoding transistors to increase the output impedance of the OTA. The basic stage consists of a common source connected transistor feeding into a common gate connected transistor, as illustrated in figure 1a. Ideally both the input transistor and the cascode transistor should be n-type, since their mobility is significantly higher than that of p-type transistors. But this places a higher demand on the voltage headroom, as more transistors have to be stacked. Since the $90nm$ CMOS technology used for this OTA required a supply voltage of no more than $1.2V$, a folded cascode architecture was chosen.

Active or "regulated" cascode gain enhancement, as seen in figure 1b, increases the cascoding effect of transistor $T2$ by using an additional gain stage. The objective is to decouple the DC gain from the unity-gain frequency of the amplifier. This means that the DC gain and the unity gain frequency (UGF) will not follow an inverse relationship, where a change in the circuit will reduce one to advance the other, as is usually the case. The feedback amplifier keeps the drain-source voltage across $T1$ as stable as possible, irrespective of the output voltage. Thus ideally increasing the output impedance by a factor equal to the gain of the added amplifier A [3].

In essence, any amplifier may be used as the additional amplifier, the simplest being a single transistor. But usually the gain enhancement OTAs are used for much of the gain and the main OTA is optimised for speed. In that case, a high gain architecture, like folded cascode, can be used for the supplemental OTAs as well.

The first implementation of the gain enhancement technique in [1] utilized single ended folded cascode amplifiers as gain enhancement amplifiers, as shown in figure 1b. Later publications [4] [5] [6] used fully differential OTAs as shown in figure 2. The DC gain enhancement remains the same, but using two fully differential amplifiers in stead of four single ended amplifiers should result in a smaller area- and power-consumption. Another advantage is a higher slew rate, since the supplemental amplifiers no longer use current mirrors in differential to single ended conversion. This reduces the dynamic performance of the main amplifier due to ringing at the output of the supplemental amplifiers [4].

Here we will present a single stage OTA which uses fully differential gain enhancement to achieve better than $60dB$ open loop DC gain and a unity gain frequency of $2.5GHz$. The architecture is shown in figure 2. The design of the OTA and the pole-zero doublet introduced by the gain enhancement are covered in section II. Section III shows the simulation results, and the conclusion follows in section IV.

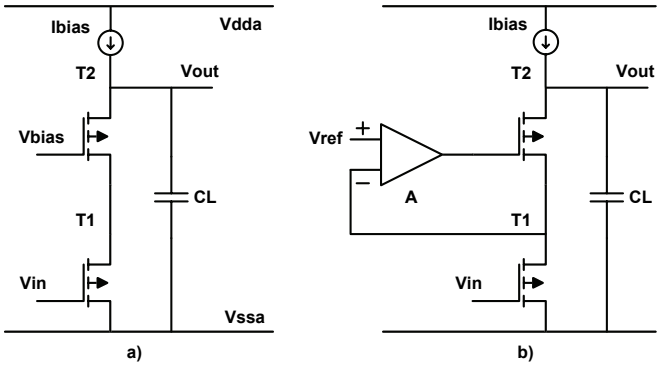

Fig. 1. (a) Regular cascode circuit. (b) Active cascode circuit.

II. Fully differential gain enhancement

The regular folded cascode architecture provided less than $40dB$ DC gain, so gain enhancement became necessary. The ADC this OTA is intended for requires a high signal swing. Thus the saturation voltage V_{dsat} of the transistors in the

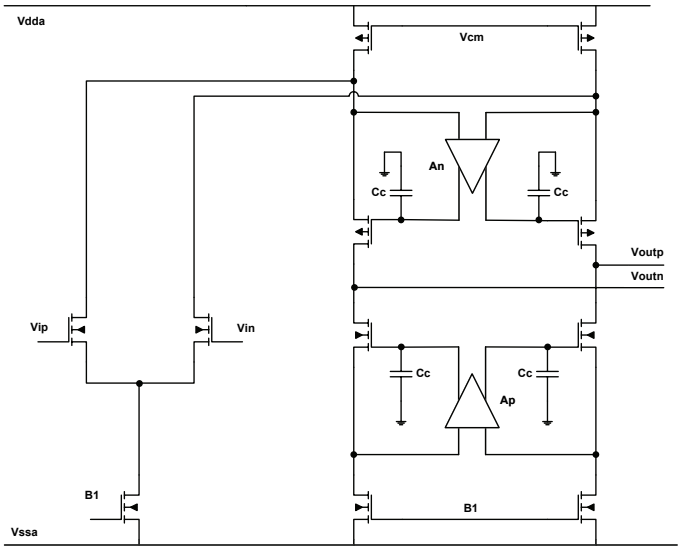

Fig. 2. OTA circuit with fully differential gain enhancement.

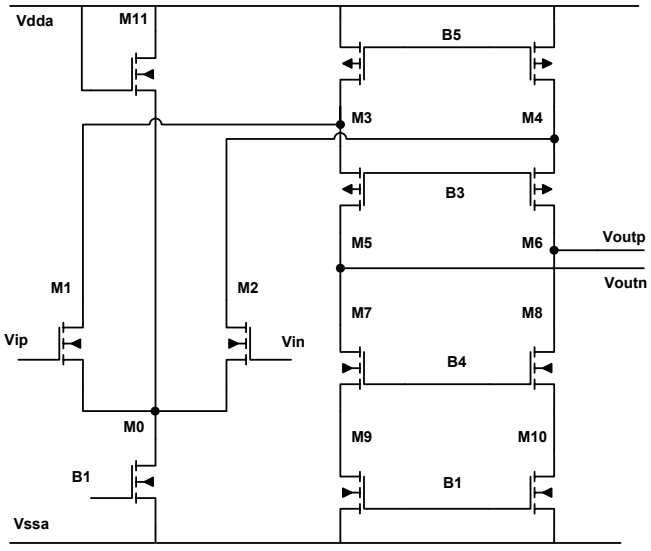

Fig. 3. Fully differential supplemental OTA .

output signal path was kept low. This presents the two gain enhancement OTAs with different common mode range requirements. For A_n the input common mode range is close to V_{dd} and thus an nmos input stage is used, like in the main circuit. Conversely A_p uses a pmos input stage. A_n is shown in figure 3.

The gain enhancement OTAs are ordinary folded cascode OTAS, except for transistor M_{11} in figure 3. This transistor serves as a single transistor common-mode feedback circuit in accordance with [4]. When a single ended output OTA is used, as in figure 1, the voltage of the drain node of $T1$ is set by V_{ref}. When fully differential OTAs are used, the voltage is set by the output DC level of the gain enhancement OTAs. Since they are connected in negative feedback, the output DC level can be set by setting the input DC level. This is done by using M_{11} to regulate the voltage at the source of the input differential pair [4].

According to [1] the regulated cascode architecture introduces a pole-zero doublet at a frequency below the unity gain frequency of the main OTA.

The doublet is a problem because it introduces a slow settling component to the amplifier. Pushing the pole-zero frequency (ω_{pz}) above the UGF of the main amplifier would remove the slow settling component regardless of the closed loop configuration. This could be achieved at the expense of a high power consumption. But the impact of the pole-zero doublet can be reduced even if it remains below the UGF, depending on the desired feedback configuration. In [1] it is shown that the frequency of the doublet needs to uphold equation (1). Thus the UGF of the supplemental OTAs ($\omega_{ugf_{supl}}$) does not need to be as high as that of the main OTA (ω_{ugf}).

$$\frac{1}{\omega_{pz}} < \frac{1}{\beta\omega_{ugf}} \tag{1}$$

Equation (1) means that the time constant of the pole-zero doublet must be smaller than the main time constant of the closed loop, where β is the feedback factor. For stability reasons, the UGF of the gain enhancement OTAs should not be above the second-pole frequency (ω_{p2}) of the main OTA. This leads to equation (2), from [1], which defines the safe range within which the UGF of the gain enhancement OTAs should be kept.

$$\beta\omega_{ugf} < \omega_{ugf_{supl}} < \omega_{p2} \tag{2}$$

The pole-zero pair also has a certain mismatch in their respective frequencies. The effects of pole-zero doublets on settling time has been presented in detail by [7]. They point out that to reduce the effects of the pole-zero doublet on both settling time and the frequency response, the spacing should be kept as low as possible.

The doublet spacing is improved by adding load capacitances to the output nodes of the supplemental OTAs [8]. The loads should not be chosen too high, since they reduce the UGF of the supplemental OTAs. Choosing higher loads will also result in a lower input referred noise level, increasing the signal to noise ratio. In this design $C_c = 1pF$ loads were necessary to reduce the pole-zero spacing and improve the frequency response. Still, figure 5 shows that the pole-zero doublet has a negative impact on the frequency response.

III. Simulation results

Open and closed loop simulations of the OTA were performed using the testbenches shown in figure 4. The open loop testbench models the load environment the OTA will face in a closed loop configuration. Hence a second device-under-test is connected at the output nodes, since the OTA (DUT) will sense the input capacitance as an added load. The closed loop testbench is straight forward except that an initial condition argument is used in the simulator to set the input common mode voltage.

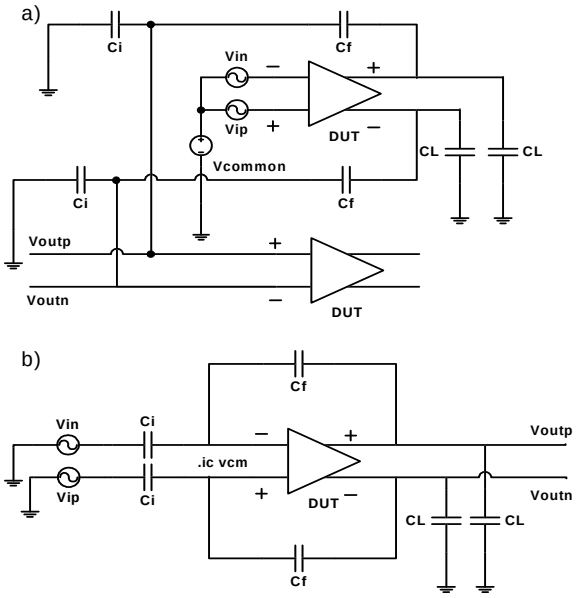

Fig. 4. (a) Open loop testbench used to simulate the frequency response. (b) Closed loop testbench used to simulate settling.

The open loop testbench showed a DC gain higher than $60dB$ with a $1V_{p-p}$ differential output swing, even when taking process corners and mismatch into account. The load is $300fF$ and the power consumption is kept below $20mW$, about 25% of which is due to the gain enhancement OTAs. For typical transistors the DC gain remained above $70dB$ at full swing.

Figure 5 shows the open loop Bode plot with and without gain enhancement. The DC gain shown here is higher than reported, since this is an AC simulation, where no signal swing is taken into account. The phase margin for unity-gain feedback shown in figure 6 is $60\,^{\circ}$, but is improved when the OTA is applied in a closed loop setup.

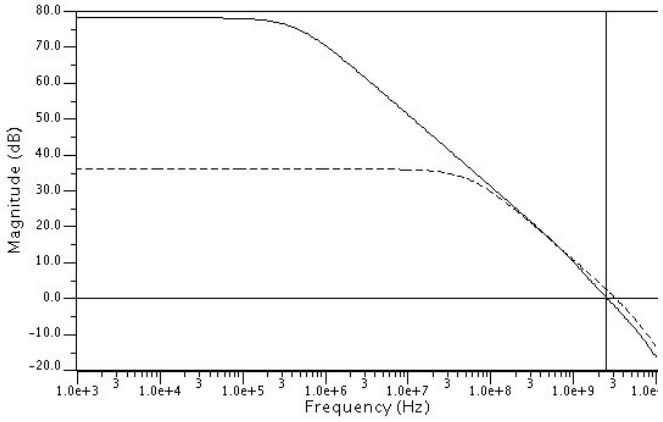

Fig. 5. Open loop Bodeplot with and without gain enhancement, showing the amplitude.

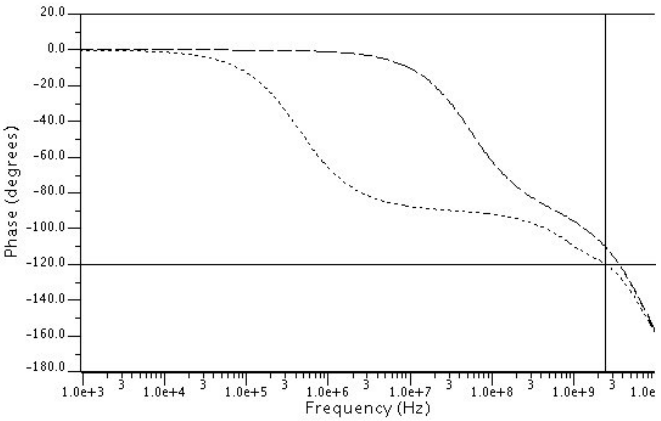

Fig. 6. Open loop Bodeplot with and without gain enhancement, showing the phase.

The unity gain frequencies of the gain enhancement OTAs were chosen as dictated by equation (2). Since the load capacitors of the gain enhancement OTAs are usually smaller than that of the main OTA, it is usually easy to design them to be fast. This is not the case here. The load capacitors of the supplemental OTAs are actually comparable to that of the main ota.

To make sure the pole-zero doublet does not impact the settling time of the OTA, the pole-zero frequency was placed above $\frac{\omega_{ugf}}{2}$ in accordance with equation (1) from [1], since β in our application is $\frac{1}{2}$.

The impact on settling time was checked by first simulating the closed loop settling time of the OTA without gain enhancement and then comparing the results to those where gain enhancement is used. This showed that the settling time remained unaffected by the gain enhancement. The OTA settles to an accuracy of 0.1% in less than $1ns$.

The simulation results of the designed OTA for typical transistors at room temperature are summarised in table I. The results are with $\pm 250mV$ output swing and $300fF$ load.

Gain enhancement	*On*	*Off*
DC Gain	$70dB$	$30dB$
UGF	$2.5GHz$	$3.1GHz$
Phase margin	$60\,^{\circ}$	$63\,^{\circ}$
Signal swing	$\pm 250mV$	$\pm 250mV$
Supply voltage	$1.2V$	$1.2V$
Slew rate	$2.5V/ns$	$2.5V/ns$
SNR	$> 60dB$	$> 60dB$
Power consumption	$< 20mA$	$< 15mA$

TABLE I

SUMMARY OF SIMULATIONS RESULTS

IV. Conclusion

This paper presented the design of a high-speed, high gain OTA in a digital $90nm$ CMOS technology. The OTA was made to use the gain enhancement technique outlined in [1]. The amplifier is fully differential an utilizes fully differential gain enhancement OTAs. Simulation results showed that for typical transistors, a DC gain of $70dB$ and a unity gain frequency of $2.5GHz$ is achieved with a $300fF$ load and $\pm 250mV$ output swing. When process corners and mismatch are taken into account, the DC gain remains above $60dB$. The circuit draws $20mA$ from a $1.2V$ power supply.

References

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