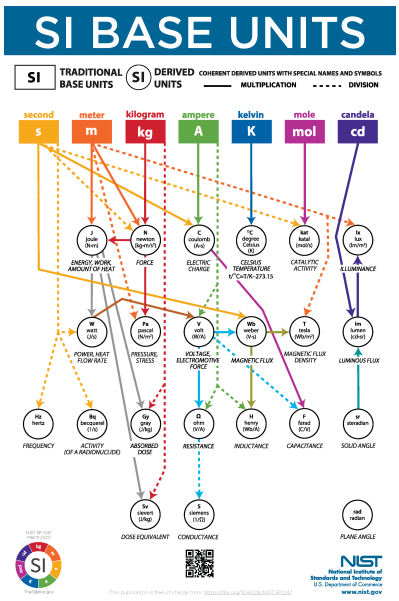
Digital to analog conversion

Carsten Wulff, carsten@wulff.no

Processing of signals has shifted into the digital domain. But the real world is analog. In order to interact with the analog we need to convert the digital signals (discrete-value, discrete-time) back to analog signals (continuous value, continuous time).

The SI base units define the fundamental analog quantities as second, meter, kilogram, ampere, kelvin, mole and candela (). Assume that electronic circuits interact with the real world in terms of second and ampere.

Related to Ampere we have the derived units of charge (Ampere Seconds), Volt (W/A), Ohm (V/A), or indeed Simens (1/Ω).



As such, to create a digital to analog converter, we somehow have to create a circuit that has a function of

$$I_{out} = D_{in} \times I_{ref} \text{ [I]}$$

$$t_{out} = D_{in} \times t_{ref} \text{ [s]}$$

$$Q_{out} = D_{in} \times Q_{ref} \text{ [C]}$$

$$V_{out} = D_{in} \times V_{ref} \text{ [V]}$$

$$R_{out} = D_{in} \times R_{ref} \text{ [}\Omega\text{]}$$

The digital value is dimensionless, as such, there must be a reference value

Digital to analog conversion can be indirect through the relations between voltage, resistance, current, time, inductance and capacitance.

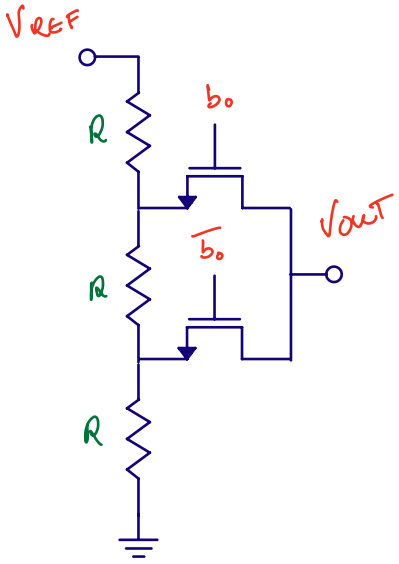
$$V = RI$$

$$Q = CV$$

$$dt = \frac{CdV}{I}$$

$$dt = \frac{LdI}{V}$$

I. Resistor based DACs

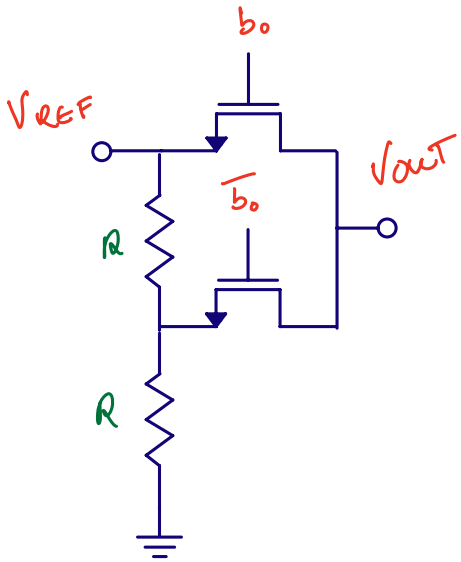


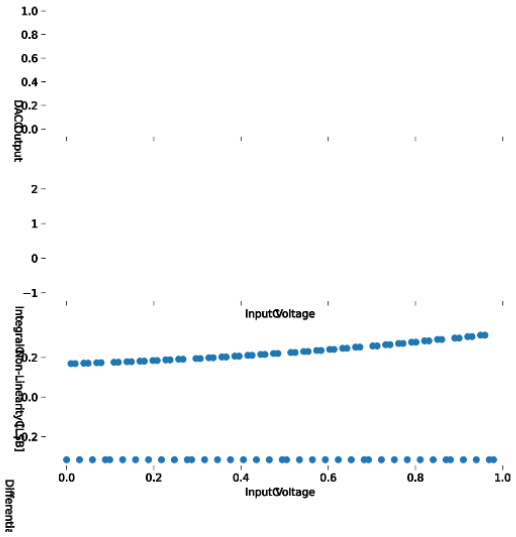
$$I_{ref} = \frac{V_{ref}}{3R}$$

$$V_{out} = D_{in} R I_{ref} = \frac{D_{in} R V_{ref}}{3R} \text{ [V]}$$

$$V_{out} = \frac{b_0 2RV_{ref}}{3R} + \frac{\overline{b_0} RV_{ref}}{3R}$$

$$V_{out} = \begin{cases} \frac{2}{3}V_{ref}, & b_0 = 1 \\ \frac{1}{3}V_{ref}, & b_0 = 0 \end{cases}$$

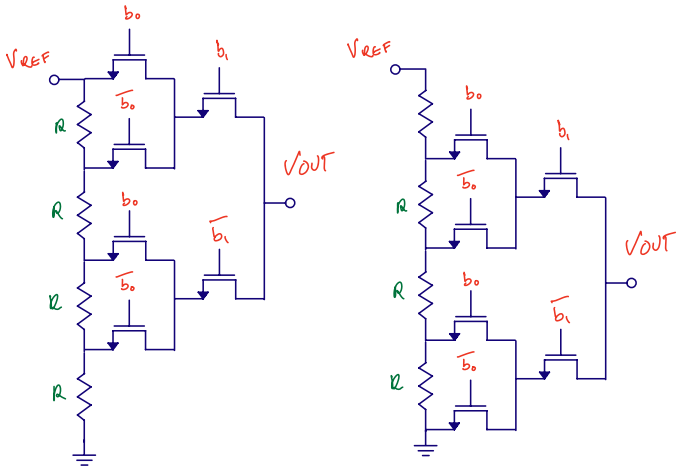


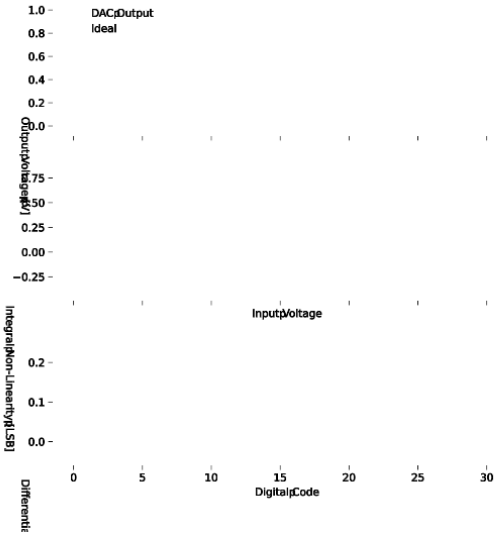


$$I_{ref} = \frac{V_{ref}}{2R}$$

$$V_{out} = \frac{b_0 2RV_{ref}}{2R} + \frac{\overline{b_0}RV_{ref}}{2R}$$

$$V_{out} = \begin{cases} V_{ref}, & b_0 = 1 \\ \frac{1}{2}V_{ref}, & b_0 = 0 \end{cases}$$





$$DNL[k] = \frac{V[k+1] - V[k]}{V_{LSB}} - 1$$

II. DAC ERRORS

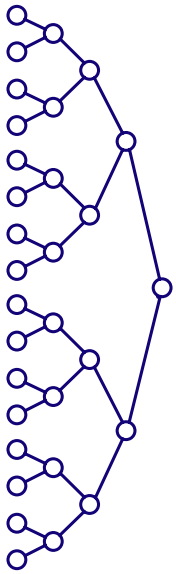
Digital to analog converters do not add quantization error. The quantization error is already in the digital word.

$$V_{out} = a_1^1 D_{in}^1 + B + \left(a_n^n D_{in}^n + ...a_2^2 D_{in}^2\right)$$

DAC output will contain gain errors, offset errors, and non-linear components

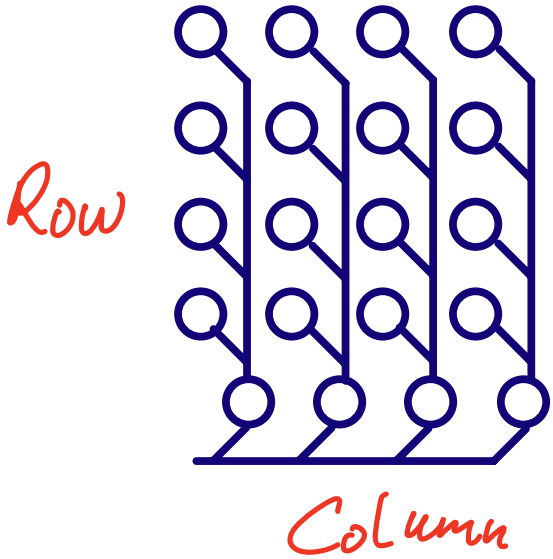
$$INL[k] = \frac{V[k] - V_{ideal}[k]}{V_{LSB}}$$

III. DAC COMPLEXITY



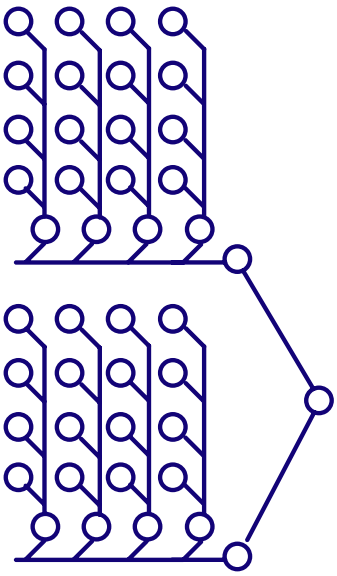
As number of resistors grow, the switches grow as

$$\sum_{n=1}^{N} 2^n = 2^{N+1} - 2$$



Use a matrix with R rows and C columns. Need R + C switches, or

$$2^N + 2^{N/2}$$



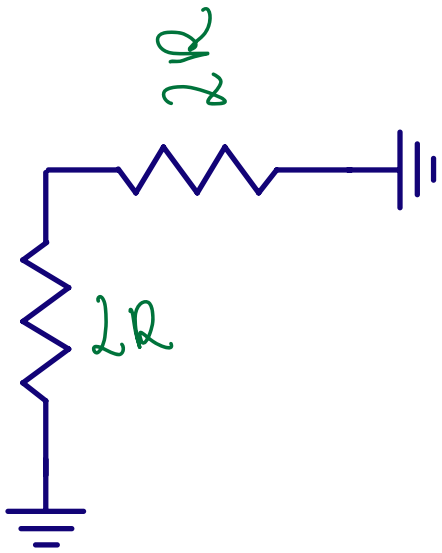
Switches in a 10-bit digital to analog converter.

Tree:	$2^{N+1} - 2 = 2046$
Matrix :	$2^N + 2^{N/2} = 1056$
6b Matrix + 4b Tree:	$2^{M+1} - 2 + 2^N + 2^{N/2} = 80$

Large number of bits, will be large number of resistors and switches.

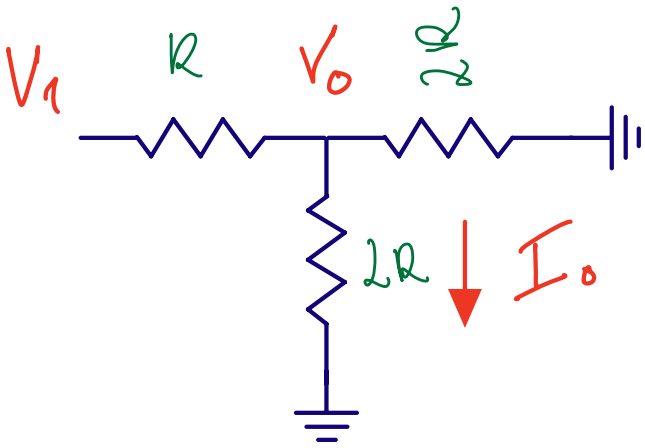
IV. BINARY SCALED DACS

$$R_{in} = 2R||2R = R$$



$$R_{in} = R + R = 2R$$

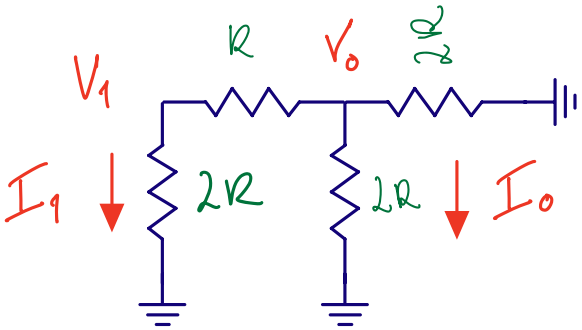
$$I_0 = \frac{V_0}{2R} = \frac{V_1}{4R}$$



$$R_{in} = 2R||2R = R$$

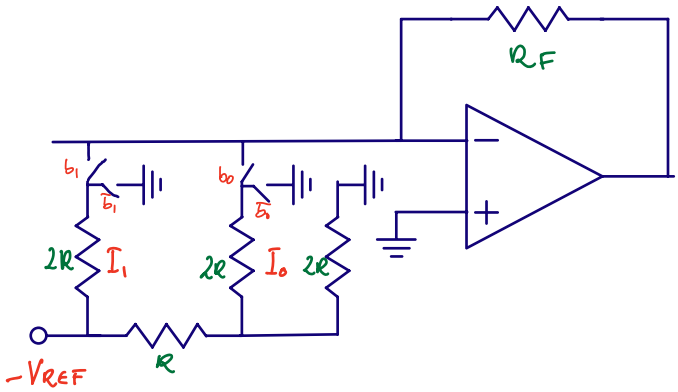
$$I_0 = \frac{V_0}{2R} = \frac{V_1}{4R}$$

$$I_1 = \frac{V_1}{2R}$$



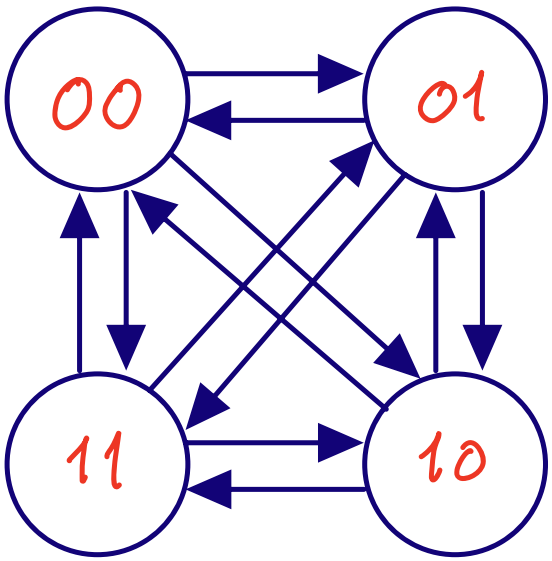
$$I_{RF} = I_1 b_1 + I_0 b_0 = \frac{V_{REF}}{2R} b_1 + \frac{V_{REF}}{4R} b_0$$

$$V_O = \left(\frac{V_{REF}}{2R} b_1 + \frac{V_{REF}}{4R} b_0 \right) R_{F0}$$



A. *Binary coding*

For 4 states (2-bit) there are 12 possible transitions



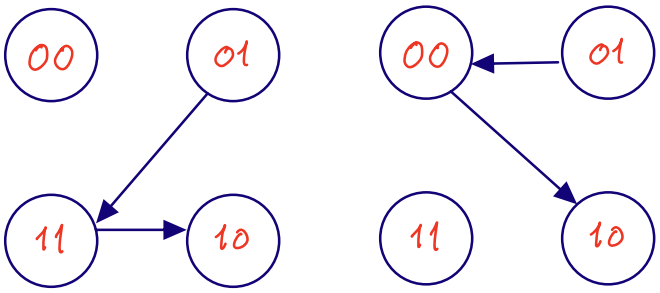
Assume MSB first (left)

$$1 \to 3 \to 2$$

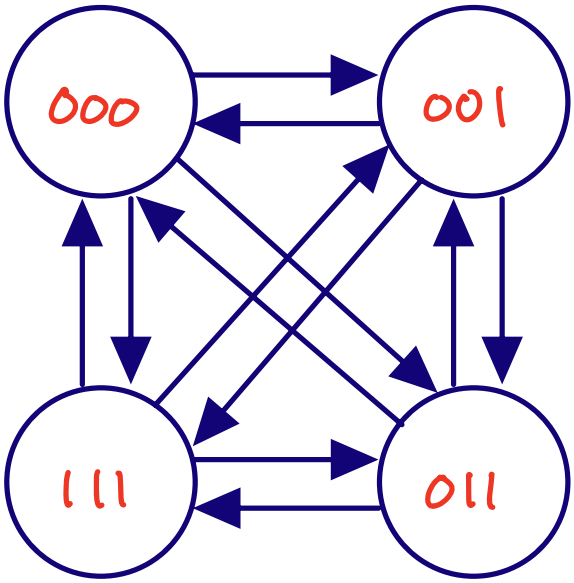
Assume LSB first (right)

$$1 \to 0 \to 2$$

Both cause a non-monotonic glitch during transition.

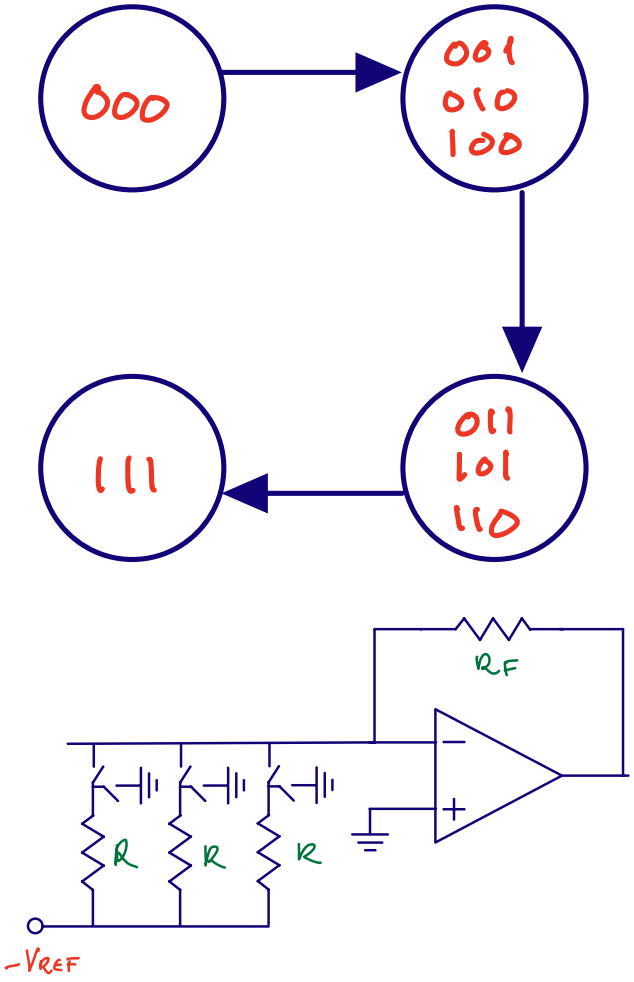


B. Thermometer encoding

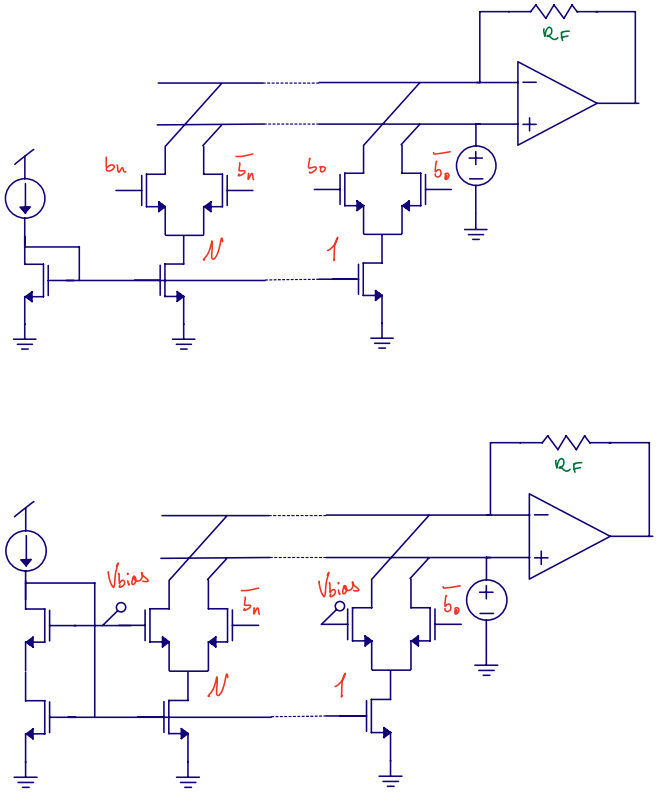


The sequence of MSB to LSB does not matter.

$$0 \rightarrow 1 \rightarrow 2 \rightarrow 3$$



V. Current mode DACs



VI. References

A 28-nm 75-fsrms Analog Fractional-N Sampling PLL With a Highly Linear DTC Incorporating Background DTC Gain Calibration and Reference Clock Duty Cycle Correction

A 10-bit Charge-Redistribution ADC Consuming 1.9 uW at 1 MS/s

A 6.3 uW 20 bit Incremental Zoom-ADC with 6 ppm INL and 1 uV Offset

A 12-Bit 1.25-GS/s DAC in 90 nm CMOS With >70 dB SFDR up to 500 MHz

Carsten Wulff received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electronics and Telecommunication, Norwegian University of Science and Technology (NTNU), in 2002 and 2008, respectively. During his Ph.D. work at NTNU, he worked on open-loop sigma-delta modulators and analog-to-digital converters in nanoscale CMOS technologies. In 2006-2007, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. Since 2008 he's been with Nordic Semiconductor in various roles, from analog designer, to Wireless Group Manager, to currently Principle IC Scientist. From 2014-2017 he did a

part time Post.Doc focusing on compiled, ultra low power, SAR ADCs in nanoscale technologies. He's also an Adjunct Associate Professor at NTNU. His present research interests includes analog and mixed-signal CMOS design, design of high-efficiency analog-to-digital converters and low-power wireless transceivers. He is the developer of Custom IC Compiler, a general purpose integrated circuit compiler, and makes the occational video on analog integrated circuits at https://www.youtube.com/@analogicus. For full CV see https://analogicus.com/markdown-cv/.