

# The Project

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*AIC is likely one of the most rewarding courses I've attended at NTNU. It gave me a lot of valuable knowledge on different types of circuits, IC design workflows and open source EDA tools that I greatly appreciate. It is also one of the most challenging courses, due to the amount of effort and time I had to spend in order to figure things out. - Tord, AIC2025*

A fantastic project/course that just might turn your world upside down, push you to re-evaluate your life choices, and stare briefly into the existential void... all while being deeply enjoyable and engaging! - Domen, AIC2025

The goal of the project is for you to experience a full mixed signal integrated circuit design, with the option of tapeout!

In 2025, two groups reached a tapeout of their design <http://analogicus.com/jnw-tt-2025/> on the <https://tinytapeout.com/chips/ttsky25a/> Tiny Tapeout shuttle.

Below is the layout of group 6 [https://analogicus.github.io/jnw\\_gr06\\_sky130a/](https://analogicus.github.io/jnw_gr06_sky130a/) and group 7 [https://analogicus.github.io/jnw\\_gr07\\_sky130a/](https://analogicus.github.io/jnw_gr07_sky130a/)

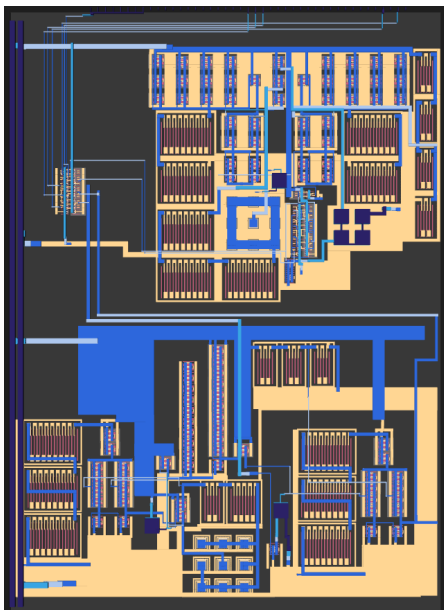


Figure 1: Layout of group 6 and group 7 temperature sensors from AIC2025

The project will walk you through the full analog/digital design process. From specification all the way to a finished layout, and a potential tapeout.

The project is not easy, it's rather hard. You'll experience frustration, desperation, epic wins, epic losses, stress, collaboration,

and you will figure out whether you love analog design, or digital design or neither.

I promise that the design project closely matches how we would develop a circuit in industry.

I ask a lot of you on the project, as such, it accounts for 45 % of the grade, and is maybe the thing that you'll learn the most from.

In this document I'll go through the problem (what we're trying to solve), and the milestones that we'll use along the way.

## I. THE PROBLEM

We want to know the temperature of the die to control complex power systems that have to adapt to high dynamic current load, and orders of magnitude change in leakage current over temperature.

1) *Complex System-on-chip have complex regulator systems:* See the example in Figure 2 from Nordic Semiconductor's nRF54L15 product specification.

VDD is the supply from the battery (1.7 V - 3.6 V). While the DECD, DECA and DECRF are the low voltage supplies for the digital, analog and radio.

The VREGMAIN has both a DC/DC, and a LDO. We'll learn about those in the course. For now it's sufficient to know that the DC/DC converts power drawn on the low supply (DECA, DECD, DECRF) to power drawn from the high supply (VDD), while the LDO has the same current on low supply as the high supply, but the voltage is different.

You will learn in the course that the typical systems inside VREGMAIN are complicated, and sometimes complex, analog circuits.

From the datasheet you'll see that the lowest power state is about 700 nA, while the highest power state is about 10 mA. The high power state is 14 thousand times higher than the low power state!

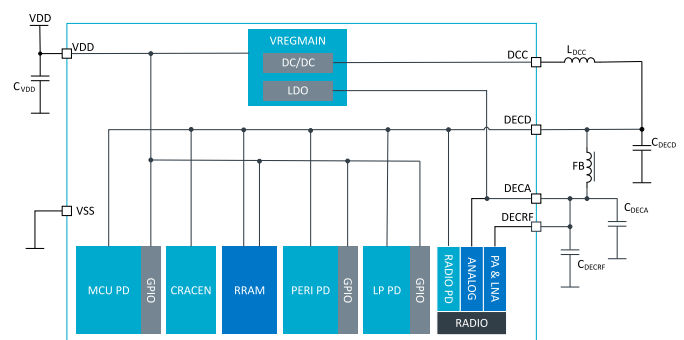


Figure 21: Regulator configuration

Figure 2: Power system of nRF54L15

2) Leakage current varies orders of magnitude over temperature: The sub-threshold leakage current in a MOSFET is

$$I_{leak} = I_0 e^{-V_{th}/nV_T} (1 - e^{-V_{ds}/V_T})$$

The change in leakage as a function of temperature is rather complicated. The  $V_T = \frac{kT}{q}$  factor is easy, but both  $I_0$  and  $V_{th}$  have a complicated relation to temperature.

In Figure 3 you can see the leakage simulation (from [http://analogicus.com/lelo\\_aic\\_sky130a/](http://analogicus.com/lelo_aic_sky130a/))

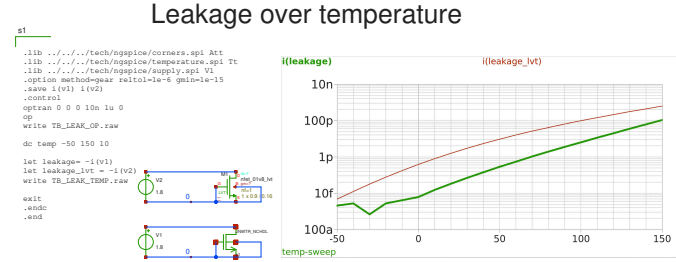


Figure 3: Leakage simulation

Based on the previous curves we could run a thought experiment.

- Assume 1 pA at 25 C, and 1 nA at 125 C, per logic cell
- Assume 100 million logic cells
- Leakage at 25 C => 100 uA
- Leakage at 125 C => 100 mA !!!

3) We would like to know the temperature on die:

- Assume we use 1 % of the load current for the regulator
- At 25 C => 1 uA
- At 125 C => 1 mA

Insanely difficult to design a regulator that is efficient across the full range.

It would be good if we could know temperature.

4) There are proposed solutions: In [1] they used a leakage based digital ring oscillator.

## II. THE PROJECT: DESIGN A TEMPERATURE SENSOR

| Parameter       | Value | Unit            | Description                                                    |
|-----------------|-------|-----------------|----------------------------------------------------------------|
| Area            | <10   | km <sup>2</sup> |                                                                |
| Conversion time | < 30  | us              | Should finish in one 32768 Hz clock period                     |
| Sample rate     | 100   | ms              |                                                                |
| Leakage current | < 1   | nA              |                                                                |
| Active current  | <     | uA              |                                                                |
| Average current | 100   | nA              | Active current x conversion time/sample rate + leakage current |
| Accuracy        | +5    | C               | One temperature (25C) calibration                              |
| Accuracy        | +1    | C               | Two temperature (25C, 85C) calibration                         |

### A. Milestone 0: The tutorial

The goal of milestone 0 is to force you to install the tools, and get

Follow: [Sky130nm Tutorial](#)

Submit link to your github repository on blackboard

For example, my repository: [LELO\\_EX\\_SKY130A](#)

**The exercise will teach you the skills you need to do the project**

### B. Milestone 1:

### C. Milestone 2:

### D. Milestone 3:

### E. Milestone 4:

### Milestone 5:

- [1] Z. Tang, Y. Fang, Z. Shi, X.-P. Yu, N. N. Tan, and W. Pan, "A 1770-  $\mu$  m<sup>2</sup> leakage-based digital temperature sensor with supply sensitivity suppression in 55-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 3, pp. 781–793, 2020, doi: [10.1109/JSSC.2019.2952855](https://doi.org/10.1109/JSSC.2019.2952855).



**Carsten Wulff** received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electronics and Telecommunication, Norwegian University of Science and Technology (NTNU), in 2002 and 2008, respectively. During his Ph.D. work at NTNU, he worked on open-loop sigma-

delta modulators and analog-to-digital converters in nanoscale CMOS technologies. In 2006-2007, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. Since 2008 he's been with Nordic Semiconductor in various roles, from analog designer, to Wireless Group Manager, to currently Principle IC Scientist. From 2014-2017 he did a part time Post.Doc focusing on compiled, ultra low power, SAR ADCs in nanoscale technologies. He's also an Adjunct Associate Professor at NTNU. His present research interests includes analog and mixed-signal CMOS design, design of high-efficiency analog-to-digital converters and low-power wireless transceivers. He is the developer of Custom IC Compiler, a general purpose integrated circuit compiler, and makes the occasional video on analog integrated circuits at <https://www.youtube.com/@analogicus>. For full CV see <https://analogicus.com/markdown-cv/>.