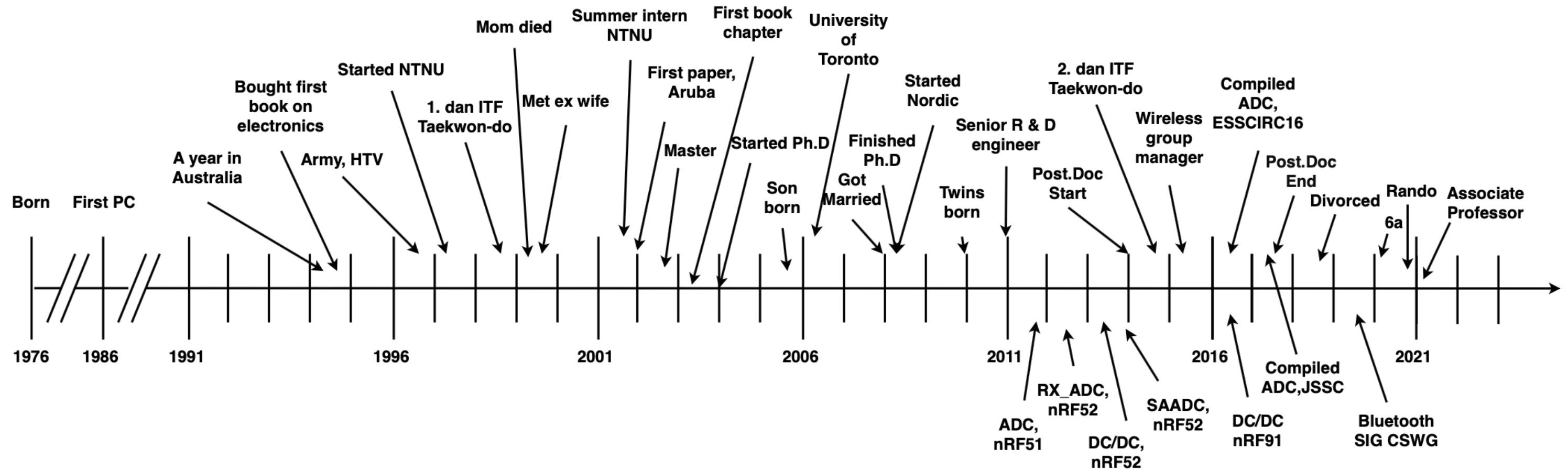


TFE4188 - Introduction to Lecture 10

Low Power Radio

Carsten Wulff



Goal

Let's make a radio (or at least, let's **pretend**)

Introduce Bluetooth

Introduce Low Power Receivers

Make the best radio ICs for gaming mice

What do we need to know?

- Data Rate
- Carrier Frequency & Range
- Power supply

Data Rate

Data

Rate

Assume 1 ms update rate

What	Bits	Why
X displacement	8	
Y displacement	8	
CRC	4	Bit errors
Buttons	16	On-hot coding. Most mice have buttons
Preamble	8	Synchronization
Address	32	Unique identifier
Total	76	

Data Rate

Application Data Rate $> 76 \text{ bits/ms} = 76 \text{ kbps}$

Assume 30 % packet loss

Raw Data Rate $> 228 \text{ kbps}$

Multiply by $\pi > 716 \text{ kbps}$

Round to nearest nice number = 1Mbps

Carrier Frequency & Range

ISM (industrial, scientific and medical) bands

6 765-6 795 kHz	(centre frequency 6 780 kHz)	FN 5.138
13 553-13 567 kHz	(centre frequency 13 560 kHz)*	FN 5.150
26 957-27 283 kHz	(centre frequency 27 120 kHz)	FN 5.150
40.66-40.70 MHz	(centre frequency 40.68 MHz)	FN 5.150
433.05-434.79 MHz	(centre frequency 433.92 MHz)in Region1**	FN 5.138
902-928 MHz	(centre frequency 915 MHz) in Region 2	FN 5.150
2 400-2 500 MHz	(centre frequency 2 450 MHz)	FN 5.150
5 725-5 875 MHz	(centre frequency 5 800 MHz)	FN 5.150
24-24.25 GHz	(centre frequency 24.125 GHz)	FN 5.150
61-61.5 GHz	(centre frequency 61.25 GHz)	FN 5.138
122-123 GHz	(centre frequency 122.5 GHz)	FN 5.138
244-246 GHz	(centre frequency 245 GHz)	FN 5.138

Antenna

Assume $\lambda/4$ is an OK antenna size ($\lambda = c/f$)

ISM band		Unit	OK/NOK
40.68 MHz	1.8	m	✗
433.92 MHz	17	cm	✗
915 MHz	8.2	cm	
2450 MHz	3.06	cm	✓
5800 MHz	1.29	cm	✓
24.125 GHz	3.1	mm	✓
61.25 GHz	1.2	mm	✓

Range (Friis)

Assume no antenna gain, power density p at distance D is

$$p = \frac{P_{TX}}{4\pi D^2}$$

Assume receiver antenna has no gain, then the effective aperture is

$$A_e = \frac{\lambda^2}{4\pi}$$

Power received is then

$$P_{RX} = \frac{P_{TX}}{D^2} \left[\frac{\lambda}{4\pi} \right]^2$$

Or in terms of distance




$$D = 10^{\frac{P_{TX} - P_{RX} + 20 \log_{10} \left(\frac{c}{4\pi f} \right)}{20}}$$

Range (Free space)

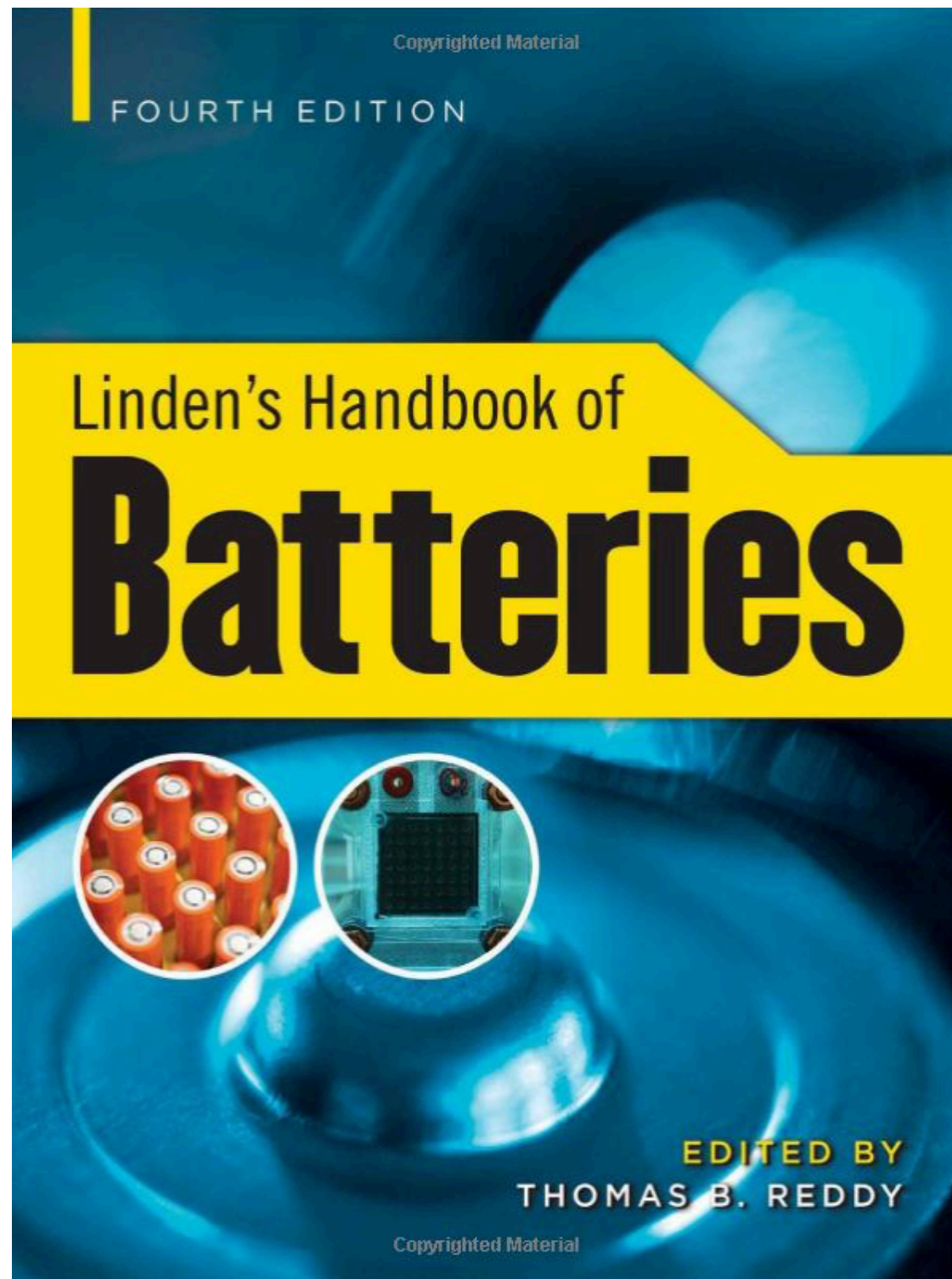
Assume TX = 0 dBm, assume RX sensitivity is -80 dBm

Freq [dB]			D [m]	OK/NOK
915 MHz	-31.7		260.9	✓
2.45 GHz	-40.2		97.4	✓
5.80 GHz	-47.7		41.2	✓
24.12 GHz	-60.1		9.9	✗
61.25 GHz	-68.2		3.9	✗
160 GHz	-76.52		1.5	✗

Path loss factor, $n \in [1.6, 6]$, $D = 10^{\frac{P_{TX} - P_{RX} + 20 \log_{10} \left(\frac{c}{4\pi f} \right)}{n \times 10}}$

Freq [dB]		D@n=2 [m]	D@n=6 [m]	OK/NOK
2.45 GHz	-40.2	97.4	4.6	
5.80 GHz	-47.7	41.2	3.45	
24.12 GHz	-60.1	9.9	2.1	

Power supply



Battery

Mouse is maybe AA, 3000 mAh

Cell	Chemistry	Voltage (V)	Capacity (Ah)
AA	LiFeS2	1.0 - 1.8	3
2xAA	LiFeS2	2.0 - 3.6	3
AA	Zn/Alk/ MnO2	0.8 - 1.6	3
2xAA	Zn/Alk/ MnO2	1.6 - 3.2	3

Decisions we must make

Modulation scheme

Scheme	Acronym	Pro	Con
Binary phase shift keying	BPSK	Simple	Not constant envelope
Quadrature phase-shift keying	QPSK	2bits/symbol	Not constant envelope
Offset QPSK	OQPSK	2bits/symbol	Constant envelope with half-sine pulse shaping
Gaussian Frequency Shift Keying	GFSK	1 bit/symbol	Constant envelope
Quadrature amplitude modulation	QAM	> 1024 bits/symbol	Really non-constant envelope

Single carrier, or multi carrier?

Bluetooth, 802.15.4, ANT all use one carrier

- Simple TX, constant envelope

WiFi, LTE ++ all use Orthogonal frequency division multiplexing (OFDM)

- Complex TX, non-constant envelope

Let's make the best, highest data rate radio!

*#*race`to`idle

Use a Software Defined Radio

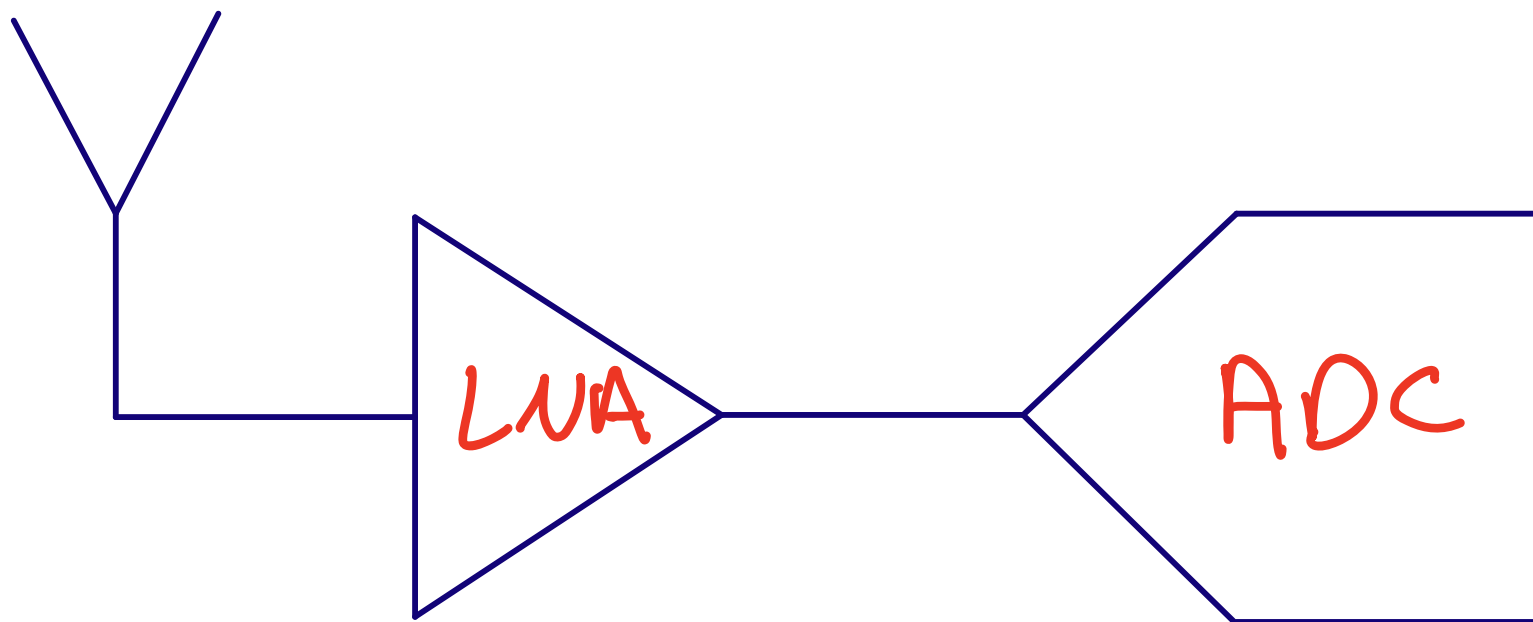
$$\text{ADC FOM} = \frac{P}{2BW2^n}$$

State of the art FOM ≈ 5 fJ/step

$$BW = 2.5 \text{ GHz}$$

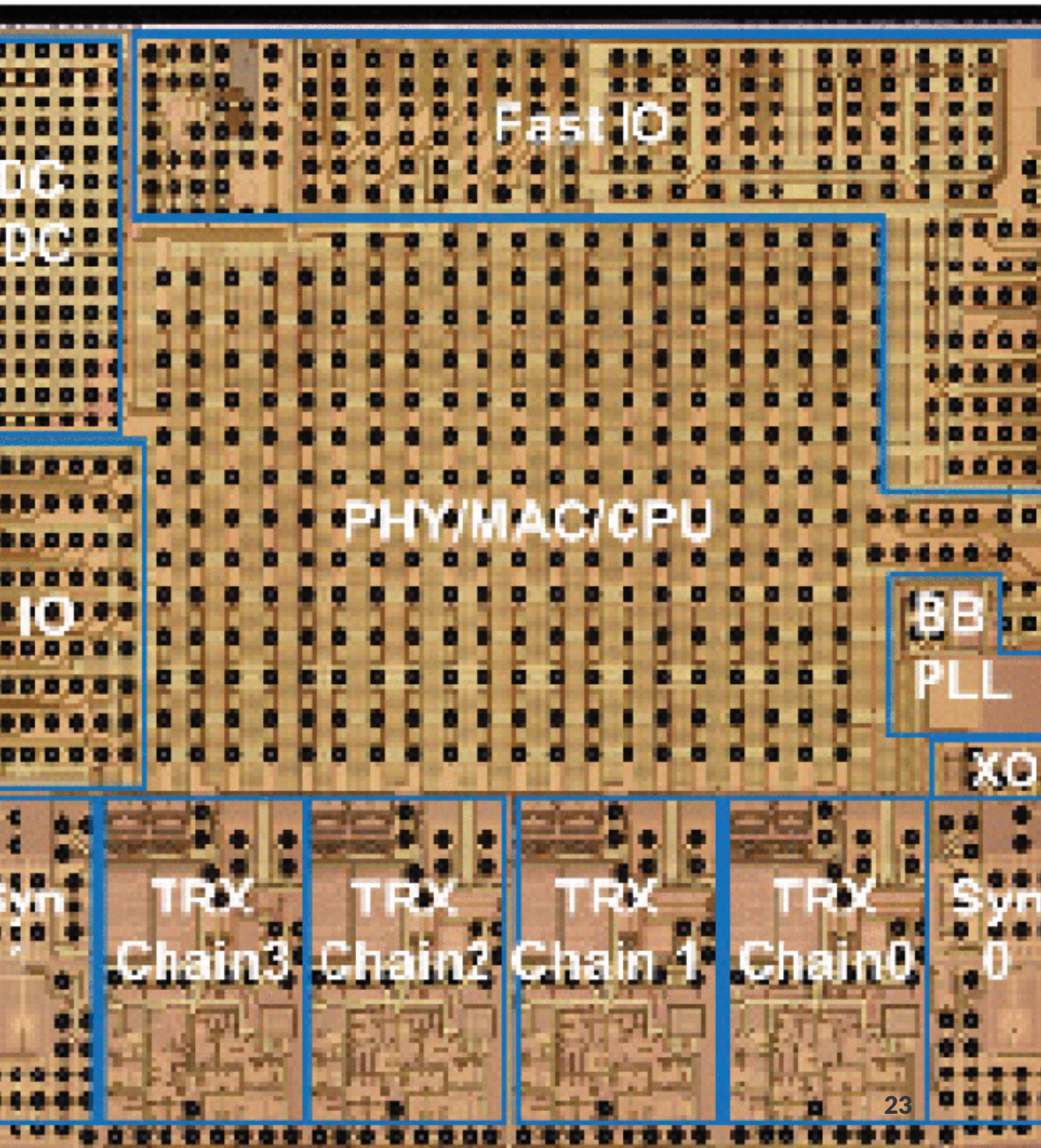
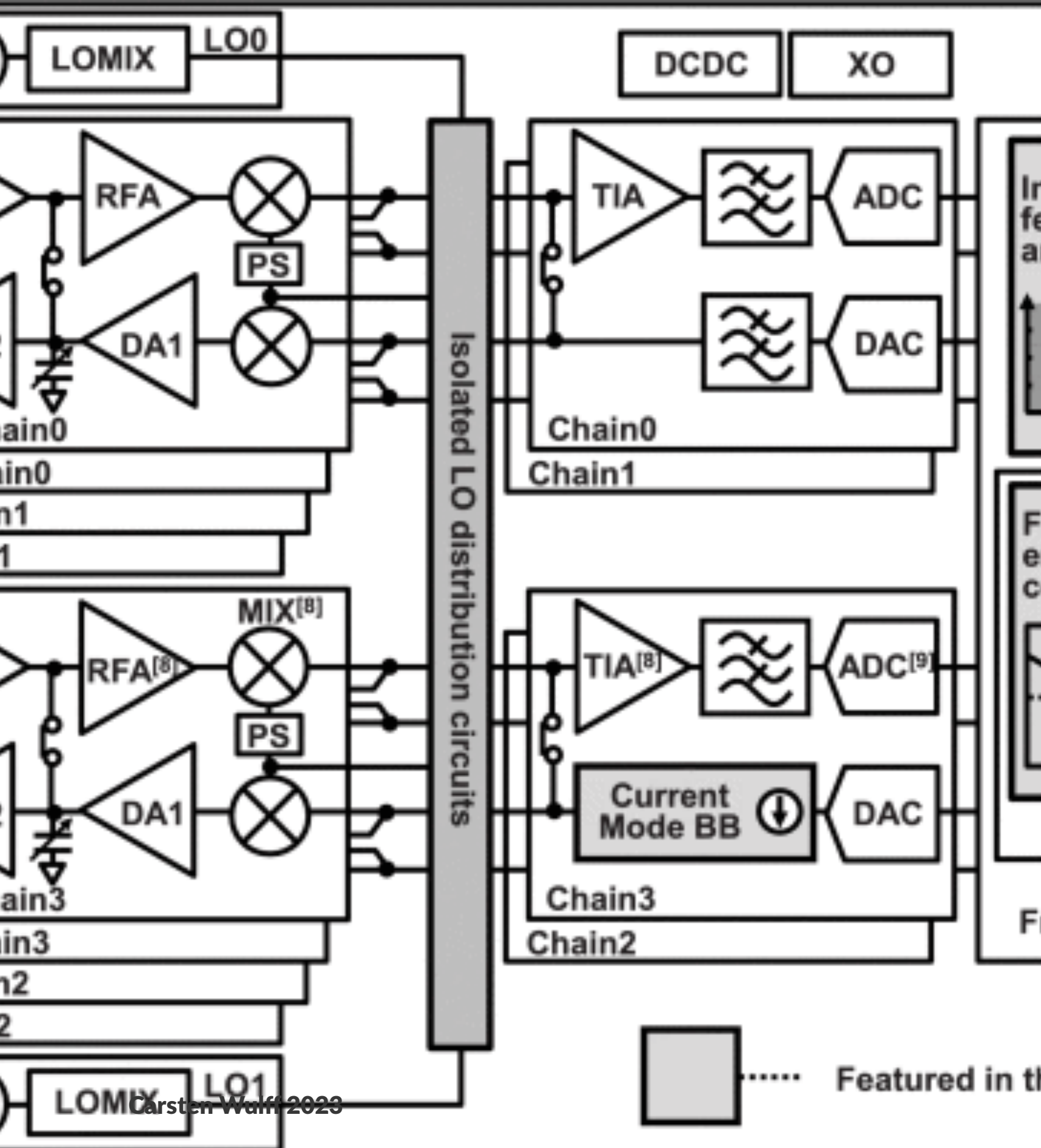
$$DR = 100 \text{ dB} = (96 - 1.76)/6.02 \approx 16 \text{ bit}$$

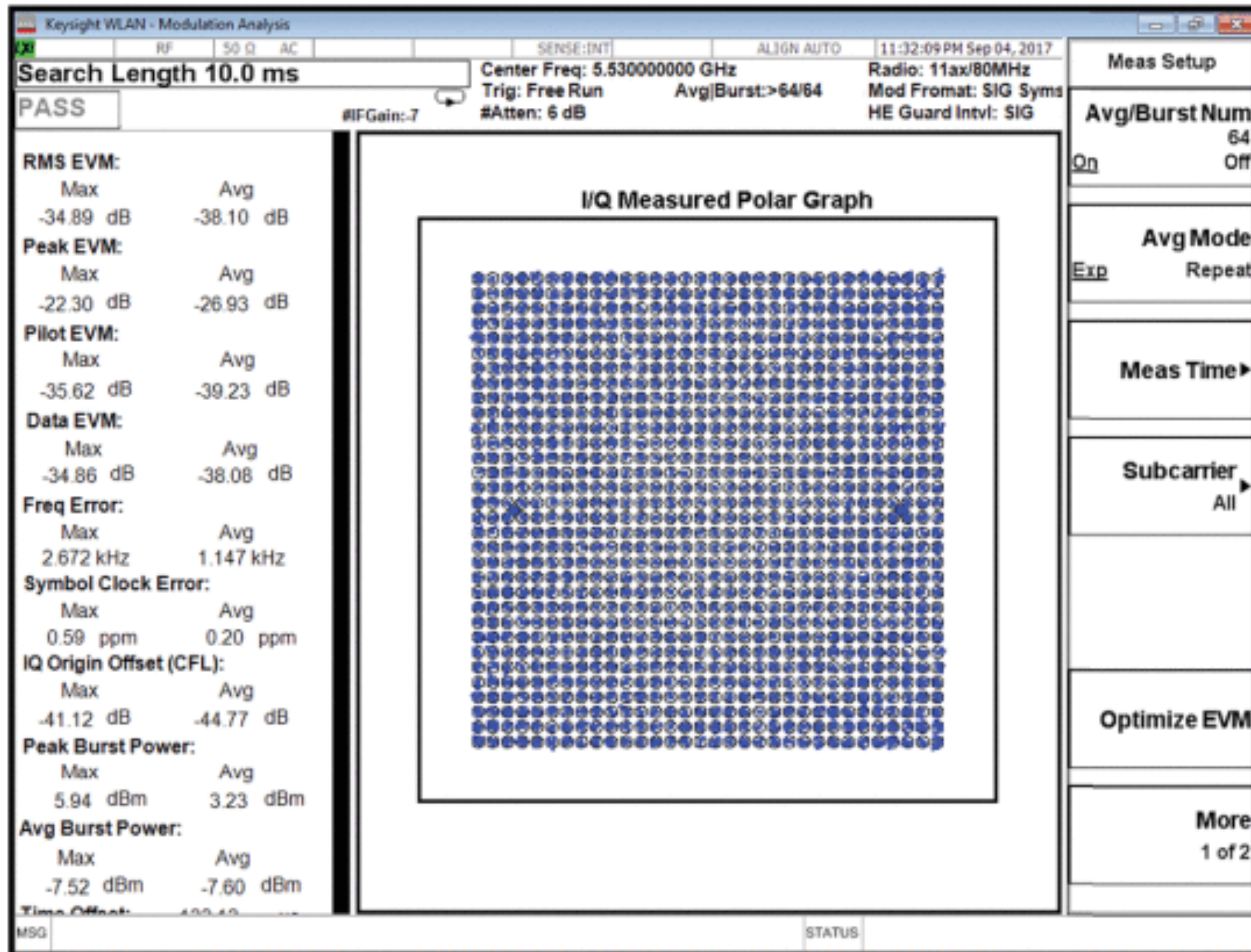
$$P = 5 \text{ fF} \times 5 \text{ GHz} \times 2^{16} = 1.6 \text{ W}$$



WiFi 6

An 802.11ax 4 × 4 High-Efficiency WLAN AP Transceiver SoC
Supporting 1024-QAM With Frequency-Dependent IQ Calibration
and Integrated Interference Analyzer





		This work	ISSCC2017[4]	JSSC2017[6]	CICC2015[3]	RFIC2014[5]	ISSCC2014[7]
WLAN standards		4x4 11abgn/ac/ax	4x4 11abgn/ac	2x2 11abgn/ac	1x1 11abgn/ac	2x2 11abgn/ac	3x3 11abgn/ac
Process [nm]		28	40	40	55	55	40
TX EVM [dB]	2.4G	-42.1(n,64QAM*3,-5dBm) -42.5(ax,40M,1KQAM*1,-5dBm)	NA	-40 (20M, Floor)	NA	-38(20M, Floor)	-41 (HT40, -5dBm)
	5G	-38.4(ac,80M,256QAM*2,-5dBm) -38.1(ax,80M,1KQAM*1,-5dBm)	-36.5(ac,80M,MCS9, Floor)	-38 (20M,Floor)	-37.8(80MHz, Floor)	-37.5(ac, 80M, Floor)	-37 (-5dBm)
RX sensitivity [dBm]	2.4G	-78.4(g,54M) -64.2(ax,40M,1KQAM*1)	-77(LG,54M)	-78.3(54Mbps)	-77.5(LG,54M)	-77.5(LG, 54M)	NA
	5G	-65.4(ac,80M,256QAM*2) -57.7(ax,80M,1KQAM*1)	-62(ac,80M,MCS9)	-66(MCS9)	-63.5(80M, MCS9)	-62.5 (ac, 80M, MCS9)	NA
RX NF [dB]	2.4G	2.9	N/A	2.9	3	3.8	3.0
	5G	3.2	N/A	4.5	3.7	4	4.3
RF power consumption [mW]	TX 2.4G	844(4SS+1LO, -5dBm)	3863 (4SS+1LO,21dBm)	1460 (2SS+1LO,20dBm)	705(1SS+1LO, 20.5dBm)	1588 (2SS+1LO, 20dBm)	1080*4 (3SS+1LO)
	TX 5G	832(4SS+2LO, -5dBm)	4164 (2SS+2LO,22dBm)	1750 (2SS+1LO,18dBm)	996 (2SS+1LO, 18.5dBm)	1722 (2SS+1LO, 17.5dBm)	1520*4 (3SS+1LO)
	RX 2.4G	354(4SS+1LO)	297(4SS+1LO)	179 (2SS+1LO)	84 (1SS+1LO)	303 (2SS+1LO)	1170*4 (3SS+1LO)
	RX 5G	447(4SS+2LO)	474(2SS+2LO)	243 (2SS+1LO)	156 (1SS+1LO)	317 (2SS+1LO)	2080*4 (3SS+1LO)
Image rejection ratio after cal. [dB]		-53(RX, Ave. over 80M) -58(RX, at 5MHz) -61(TX, Ave. over 80M) -64(TX, at 5MHz)	-61(TX,at 5MHz)	NA	-45(RX)	-45(RX)	NA
RF chip area[mm ²]		12.0	11.4	8.6	3.4*6	7.7	21.5*5
1K QAM		Yes	No	No	No	No	No
FD-IQ amp. mismatch calibration		Yes	No	No	No	No	No
Non-contiguous		Yes	Yes	No	No	No	No
Integrated interference analyzer		Yes	No	No	No	No	No

*1 Modulation and coding scheme is MCS11 *2 Modulation and coding scheme is MCS9 *3 Modulation and coding scheme is MCS7 *4 SoC power *5 SoC area *6 Including BT RF area

Crap, complex!
Crap, too high power!



Bluetooth[®]

Bluetooth

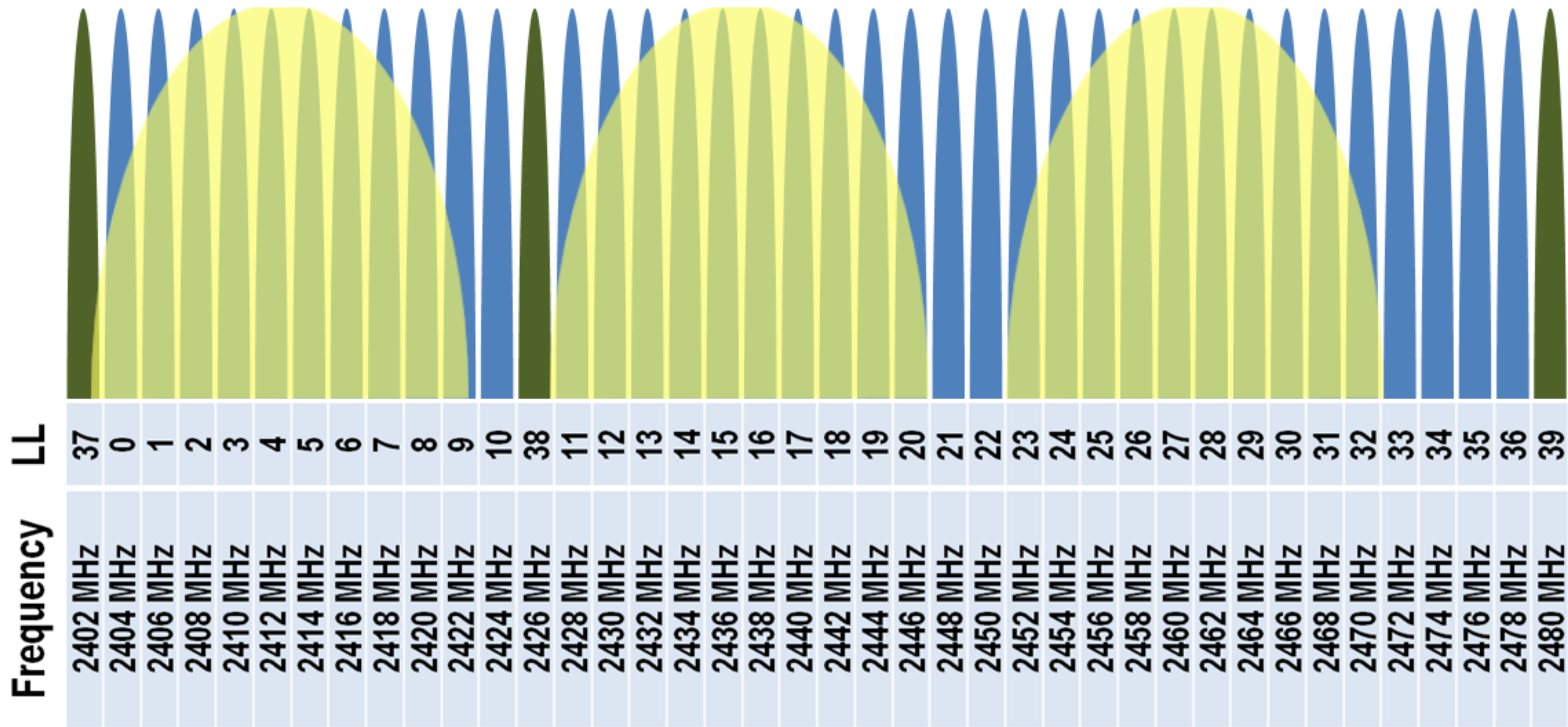
- Compromise between speed, power and cost
- "Simple" to use
- "Simple" to implement

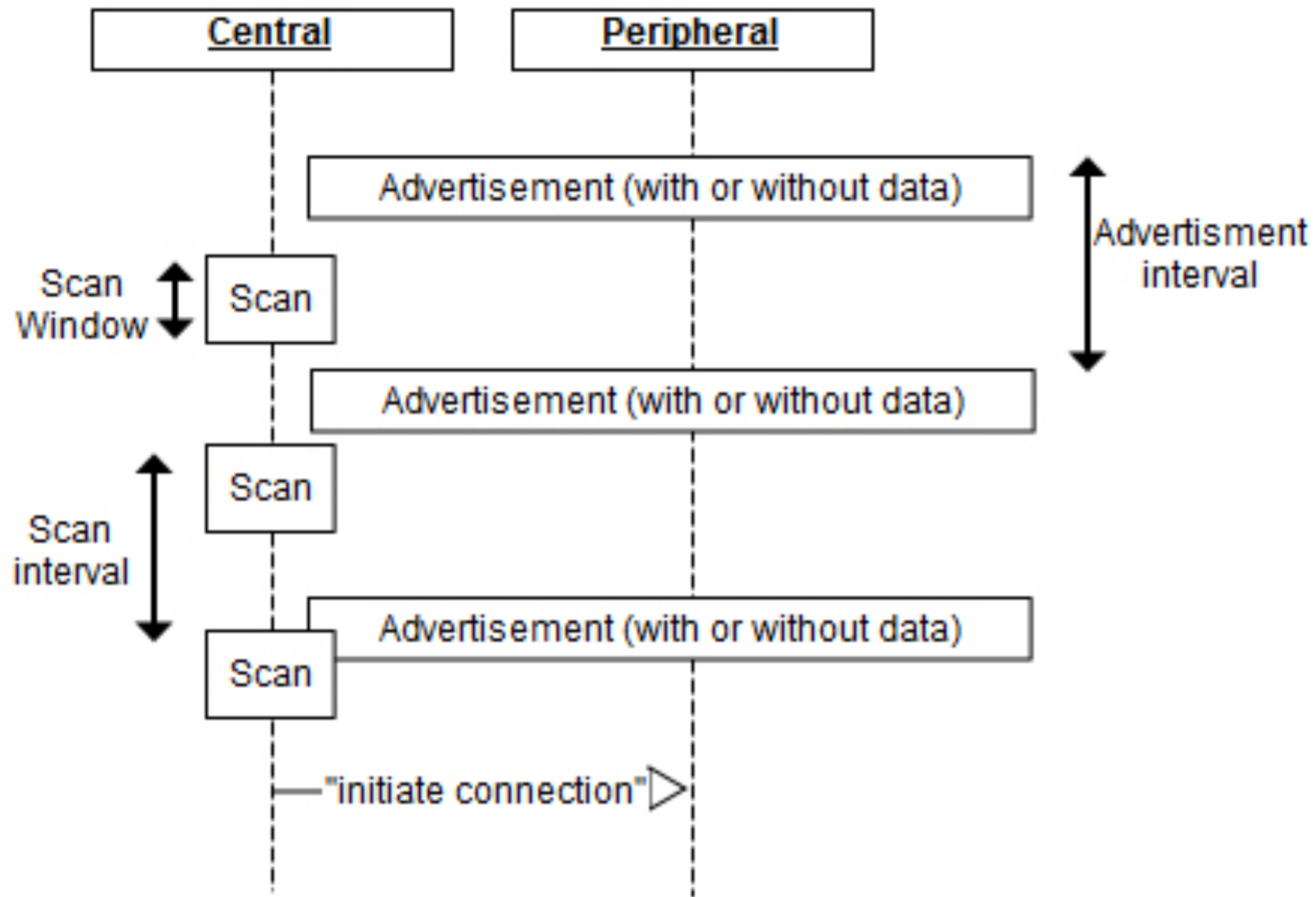
Bluetooth Basic Rate/Extended Data rate

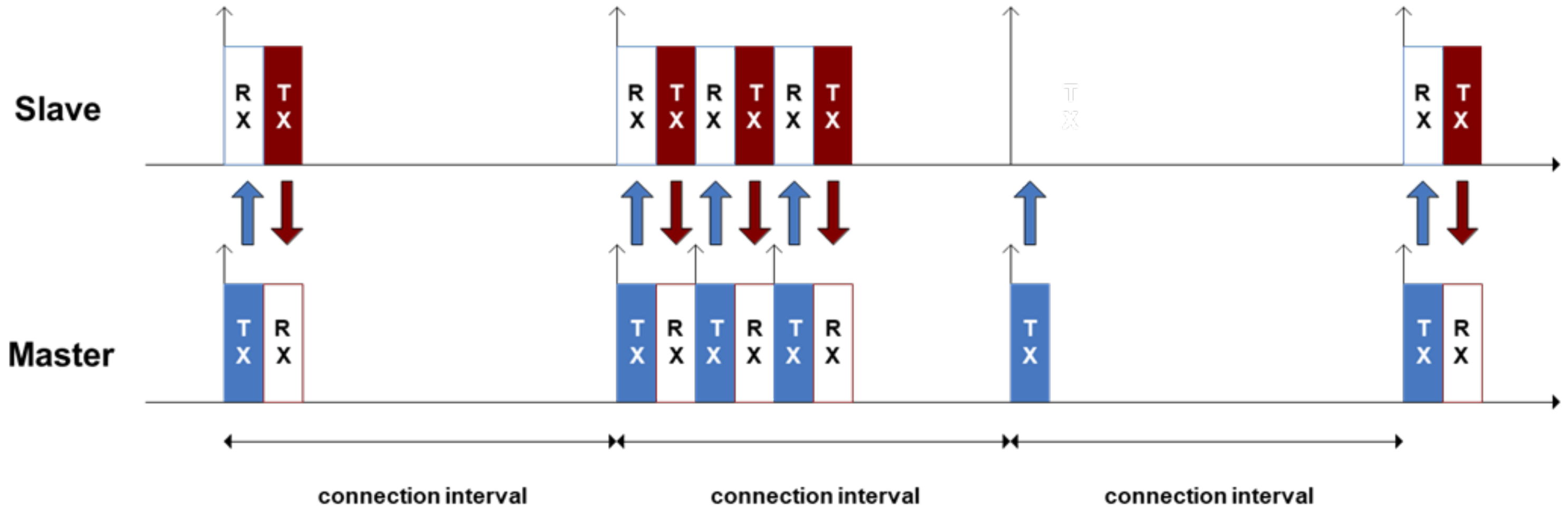
- 2.400 GHz to 2.4835 GHz
- 1 MHz channel spacing
- 78 Channels
- Up to 20 dBm
- Minimum -70 dBm sensitivity (1 Mbps)
- 1 MHz GFSK (1 Mbps), pi/4-DQPSK (2 Mbps), 8DPSK (3 Mbps)

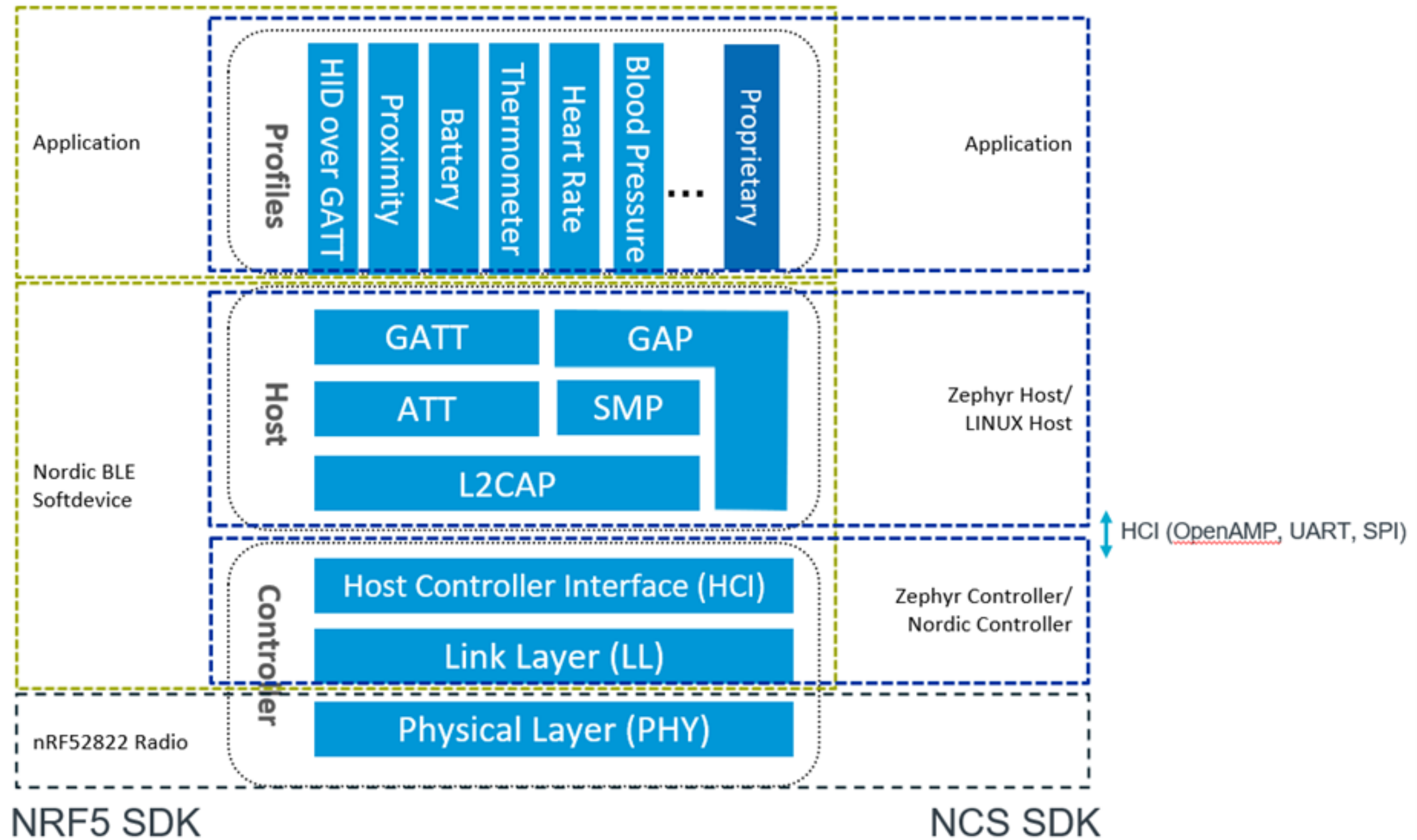
Bluetooth Low Energy

- 2.400 GHz to 2.480 GHz
- 2 MHz channel spacing
- 40 Channels (3 primary advertising channels)
- Up to 20 dBm
- Minimum -70 dBm sensitivity (1 Mbps)
- 1 MHz GFSK (1 Mbps, 500 kbps, 125 kbps), 2 MHz GFSK (2 Mbps)



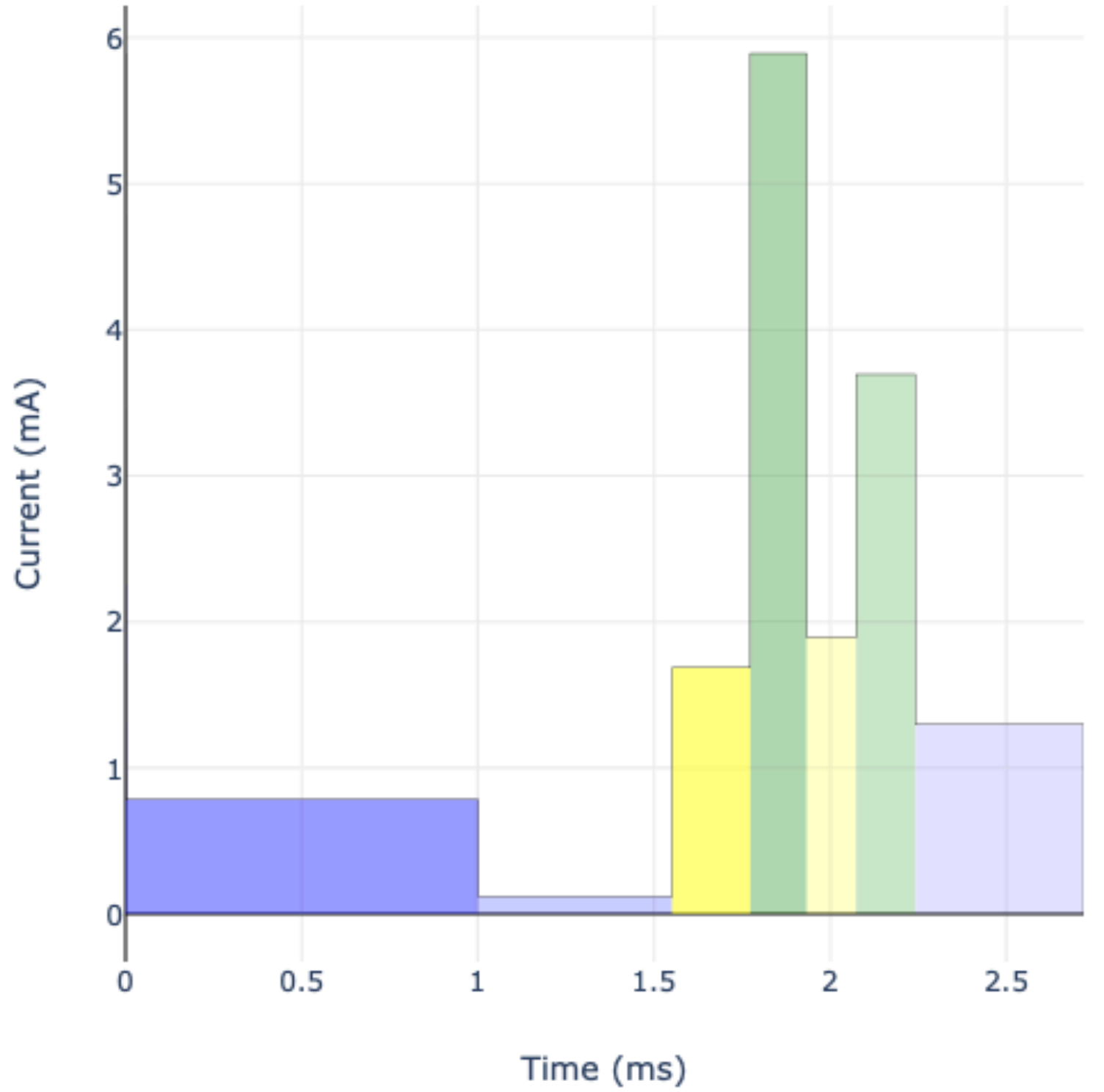






Test setup	
Voltage	3.0 V
Regulator	DCDC
Application RAM	512 kB
Network RAM	64 kB
BLE event details	
Interval	7.50 ms
Length	2.72 ms
Number of packets	1
Master sleep clock accuracy	20 ppm
Slave sleep clock accuracy	20 ppm
Data transmission	
LL PDU size	27 Byte
TX payload per event	10 Byte
TX LL throughput	10.67 kbps
RX payload per event	10 Byte
RX LL throughput	10.67 kbps
On air data rate	1 Mbps

Current consumption	
BLE event total charge	6.06 μC
Idle current	3.1 μA
Total average current	811 μA



- Pre-processing
- Standby
- Radio TX
- Radio RX
- Crystal ramp-up
- Start radio
- Radio switch
- Post-processing

For further information [Building a Bluetooth application on nRF Connect SDK](#)



Bluetooth LE in Higher Frequency Bands

A specification development project is currently underway to define the operation of Bluetooth Low Energy (LE) in additional unlicensed mid-band spectrum, including the 6 GHz frequency band. With over 5 billion products shipping each year, Bluetooth technology is the most widely deployed wireless standard in the world. A core reason for its unmatched adoption and success is the continual evolution of the technology in key areas, including higher data throughput, lower latency, and greater positioning accuracy. The new spectrum expansion project will help ensure that these Bluetooth performance enhancements can continue well into the future, paving the way for the next generation of Bluetooth innovation.

This project currently includes [enhancements being made to the Bluetooth Core Specification](#) taking place within the [Higher Bands for LE Subgroup](#) within the [Core Specification Working Group](#). Employees of all Bluetooth SIG member companies are welcome to join the subgroup to participate in the project.



Higher Data Throughput

Added to Bluetooth[®] wireless technology in 2016, the [LE 2M PHY](#) doubled the data rate that could be achieved between Bluetooth Low Energy (LE) devices from the original LE 1M PHY. The LE 2M PHY was introduced to address a number of market opportunities, including enhancing data transfer performance for the growing number of IoT devices consumers were connecting to their smartphones.

Today, an increasing number of these connected devices are looking for even greater data transfer performance, as well as support for streaming larger media, and could benefit from an even higher data rate Bluetooth LE PHY. The Higher Data Throughput project was established to address that growing market need.

This project currently includes [enhancements being made to the Bluetooth Core Specification](#) taking place within the [Core Specification Working Group](#).



High Accuracy Distance Measurement

Adding to the growing set of device positioning capabilities of Bluetooth[®] wireless technology – which currently includes Advertising (for presence), RSSI (for basic distance measurement) and [Direction Finding](#) (for high accuracy direction) – a specification development project is currently underway to enable high-accuracy distance measurement between two Bluetooth enabled devices. This feature is expected to enable the creation of locating systems that can provide even higher levels of accuracy.

This project currently includes:

- [Enhancements being made to the Bluetooth Core Specification](#) taking place within the [Core Specification Working Group](#)
- A [new profile specification](#) being developed within the [Direction Finding Working Group](#)

Low Power Receivers

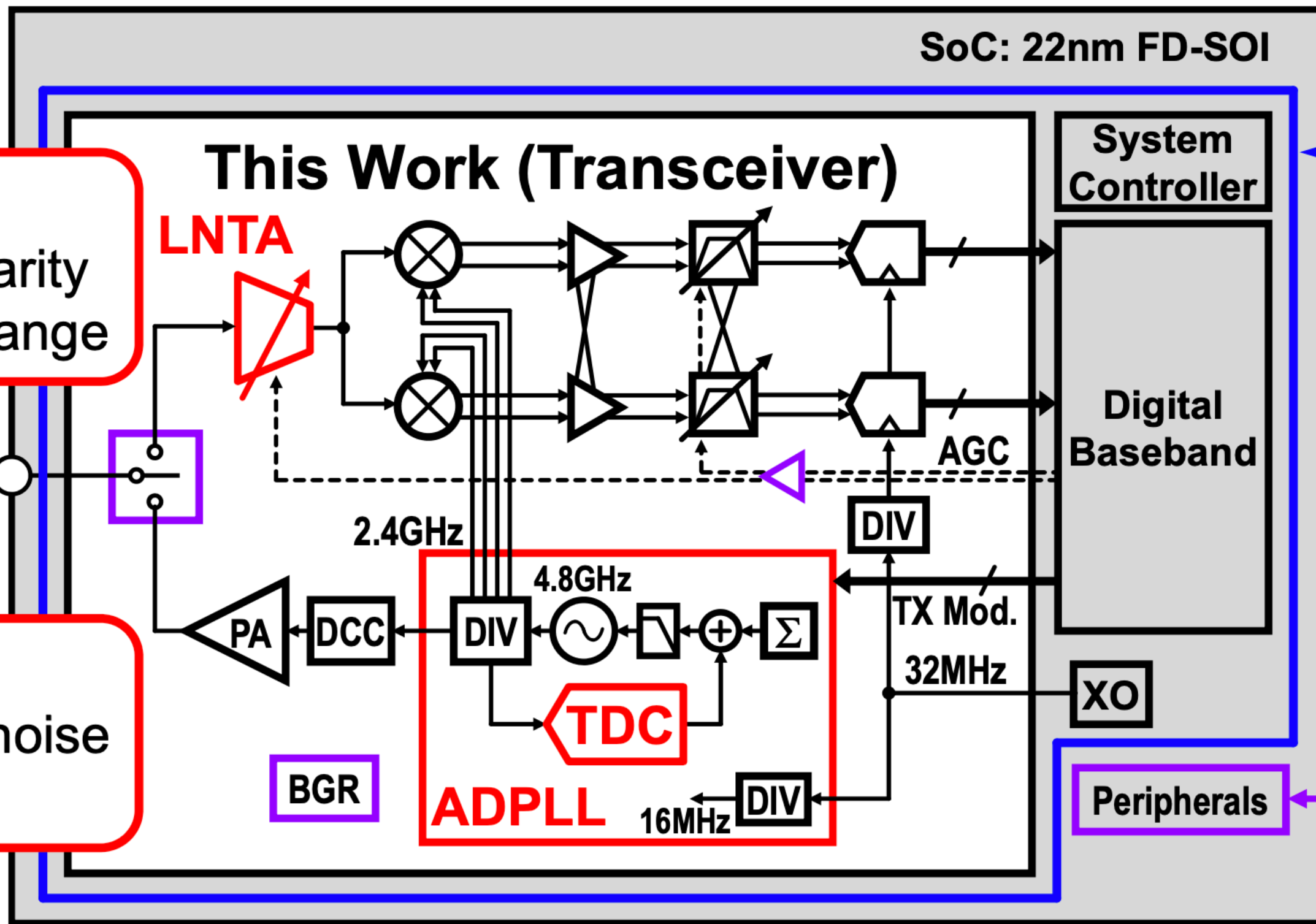
Algorithm to design state-of-the-art BLE radio

- Find most recent digest from International Solid State Circuit Conference (ISSCC)
- Find Bluetooth low energy papers
- Pick the best blocks from each paper

Design Challenges

- RX**
- High linearity
 - Wide D-range

- TX**
- Low phase noise
 - Low spur



DCC: Duty-Cycle Corrector
Carsten Wulff 2023

Blocks	Key parameter	Architecture	Complexity (nr people)
Antenna	Gain, impedance	??	<1
RF match	loss, input impedance	PI-match?	<1
Low noise amp	NF, current, linearity	LNTA	1
Mixer	NF, current, linearity	Passive	1
Anti-alias filter	NF, linearity	TIA + AFIR	1
ADC	Sample rate, dynamic range, linearity	NS-SAR	1 - 2
PLL	Freq accuracy, phase noise, current	AD-PLL	2-3
Baseband	Eb/NO, gate count, current	Verilog, but first Matlab	> 10

L N T A

MIXER

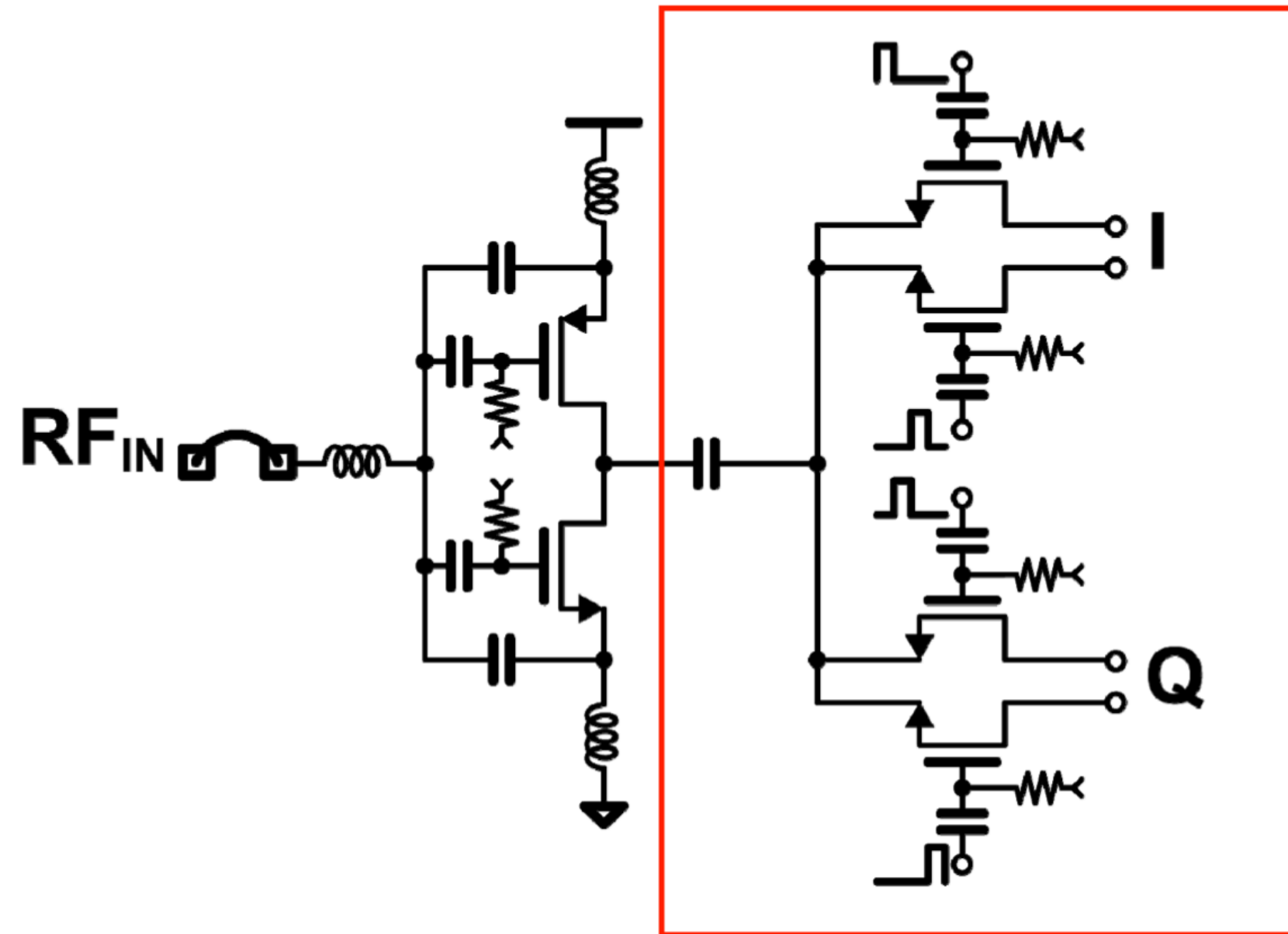
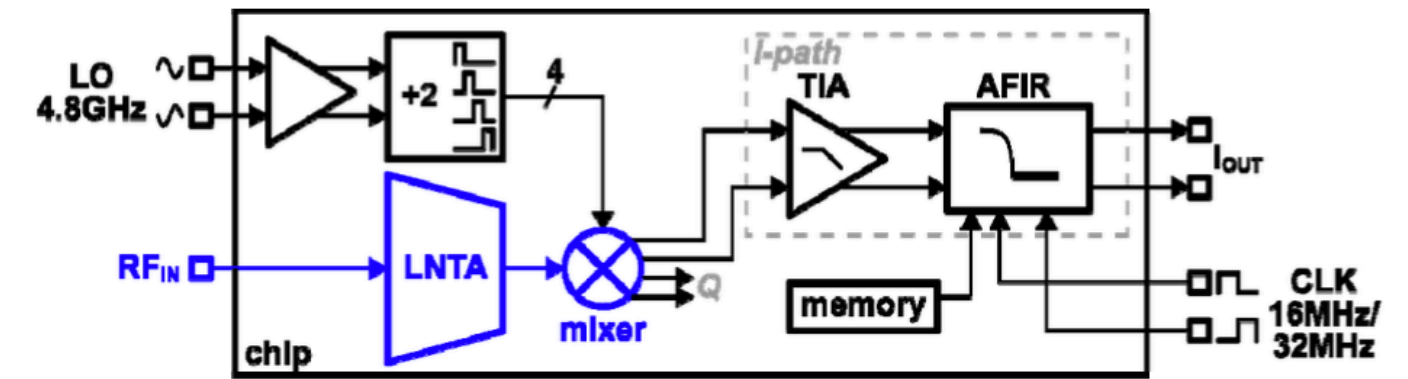
LNTA and Mixer

LNTA

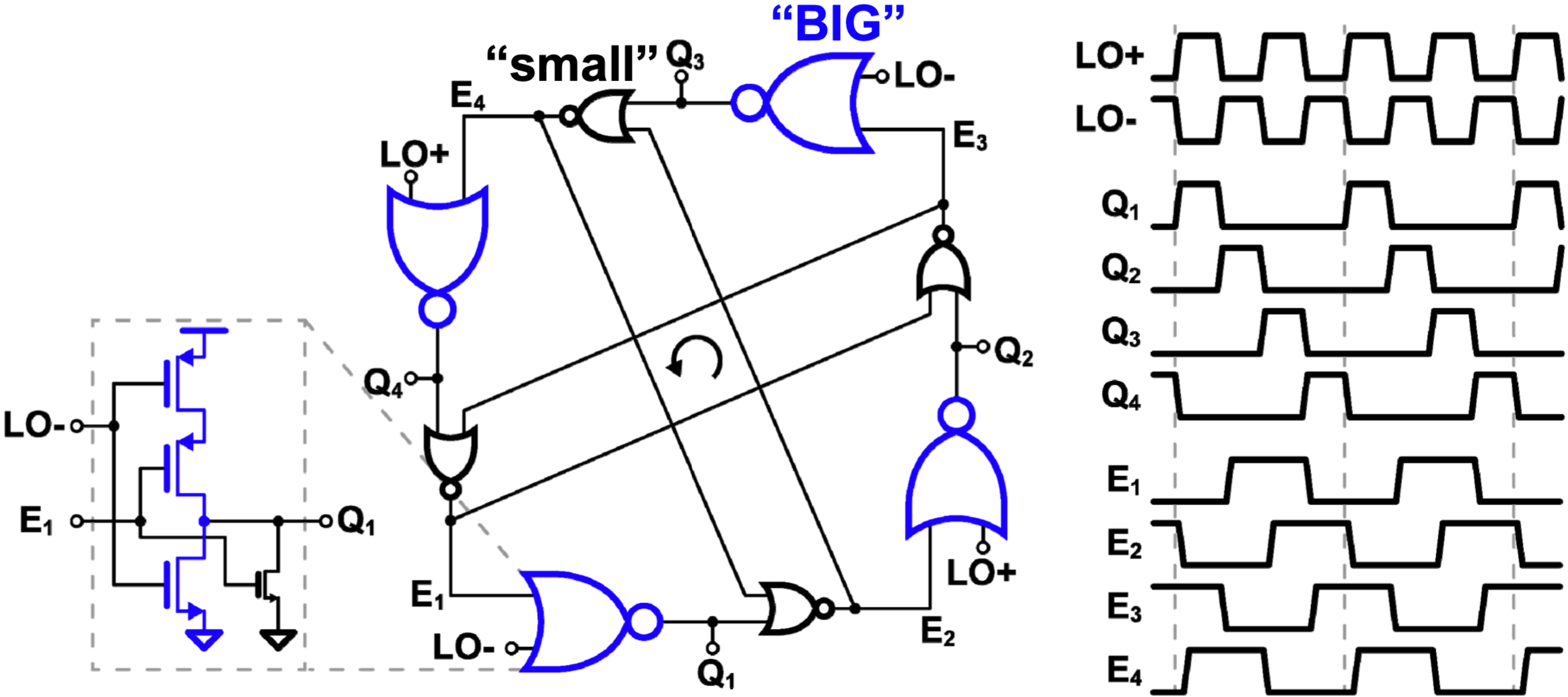
- Push-Pull
- Inductive degeneration
[Jiang, CICC'18]

Mixer

- Passive
- 25% duty-cycle clocks

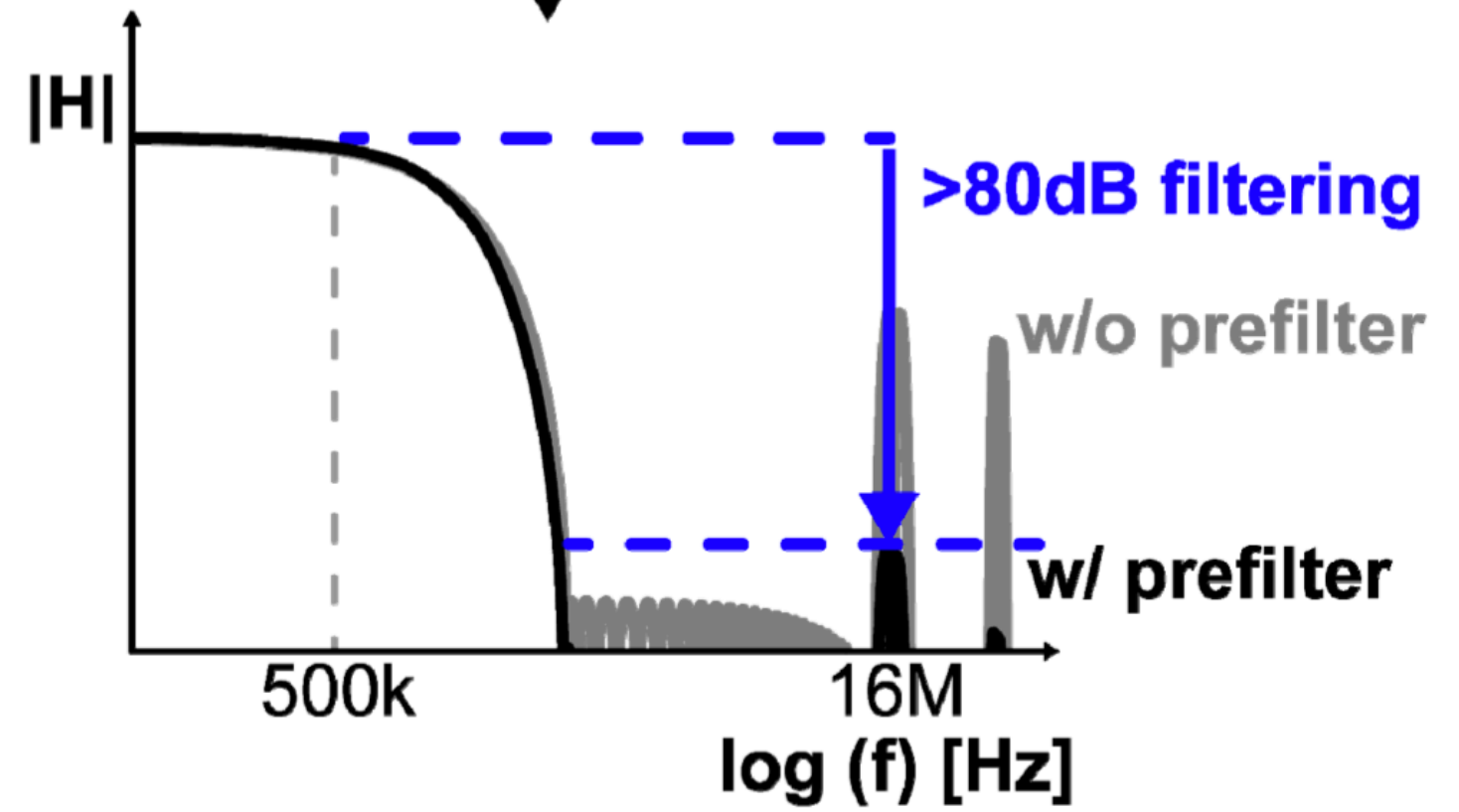
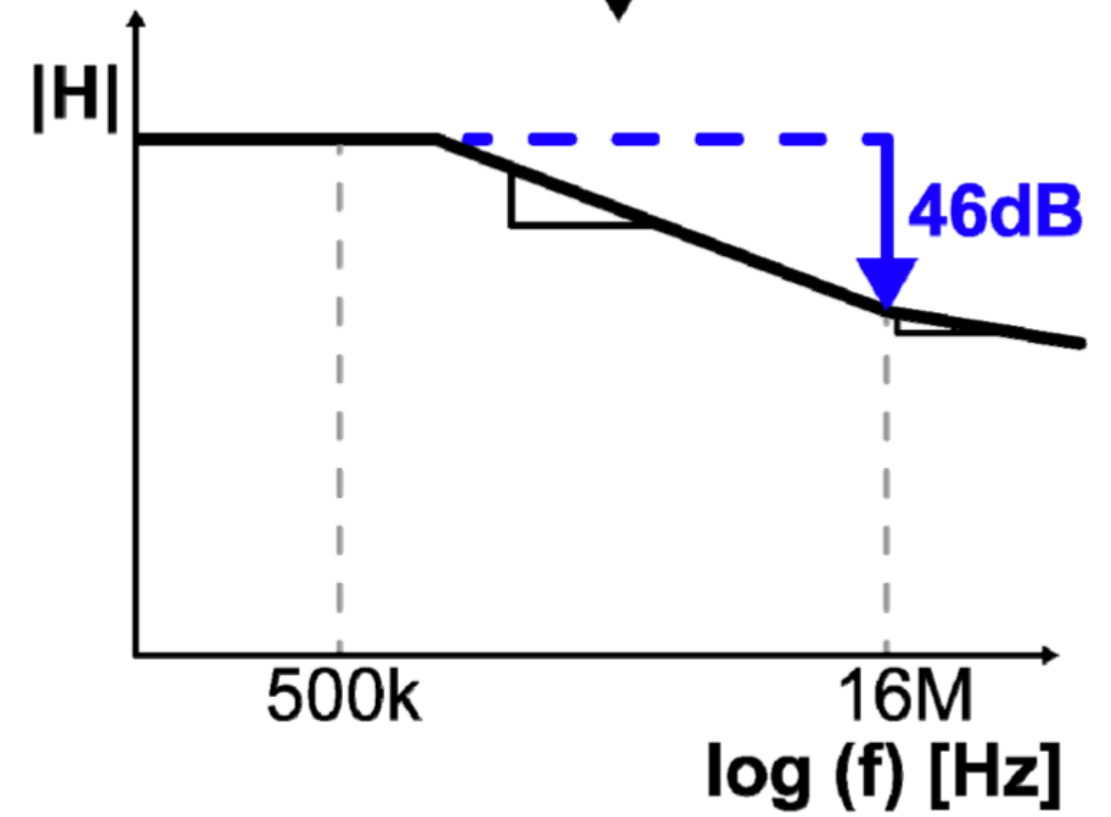
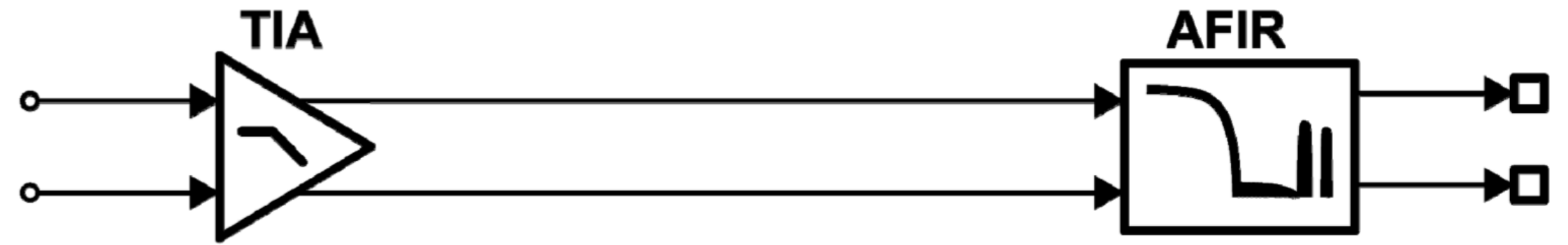
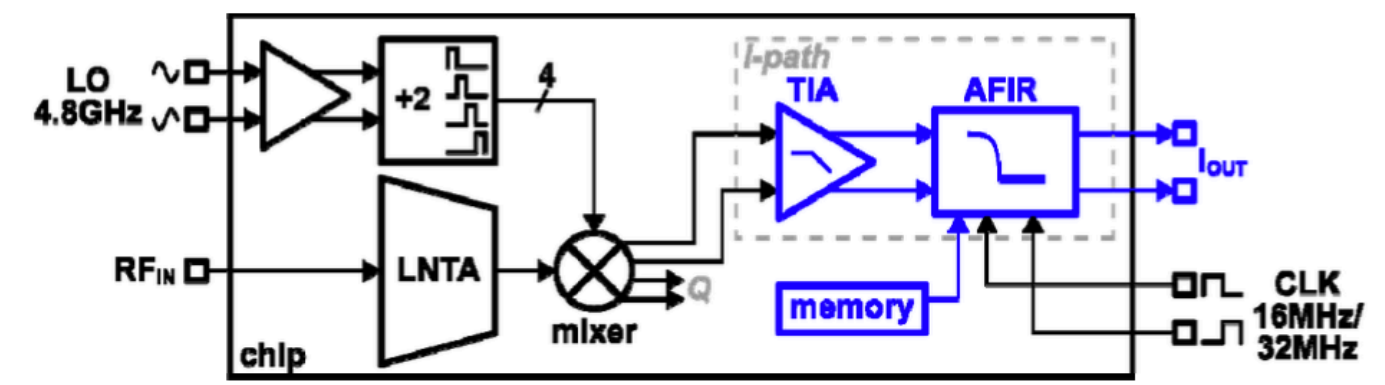


Combining and Sizing



A A F

Baseband Architecture



A D C

A Compiled 9-bit 20-MS/s 3.5-fJ/conv.step SAR ADC in 28-nm FDSOI for Bluetooth Low Energy Receivers

Carsten Wulff, *Member, IEEE*, and Trond Ytterdal, *Senior Member, IEEE*

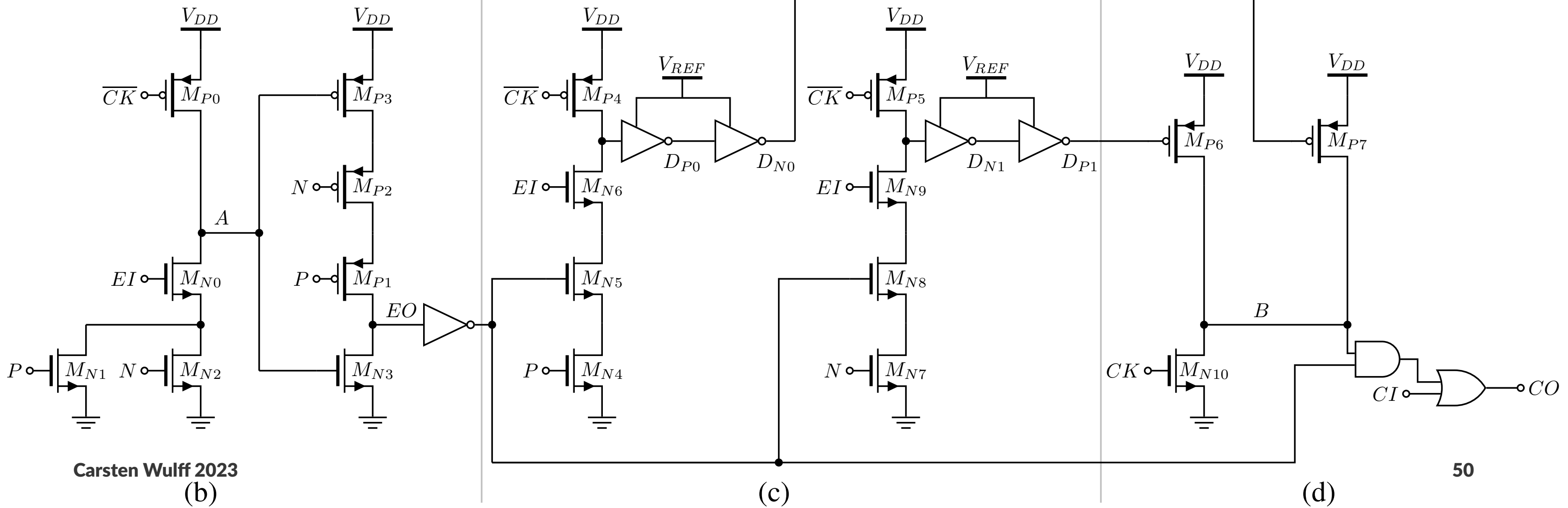
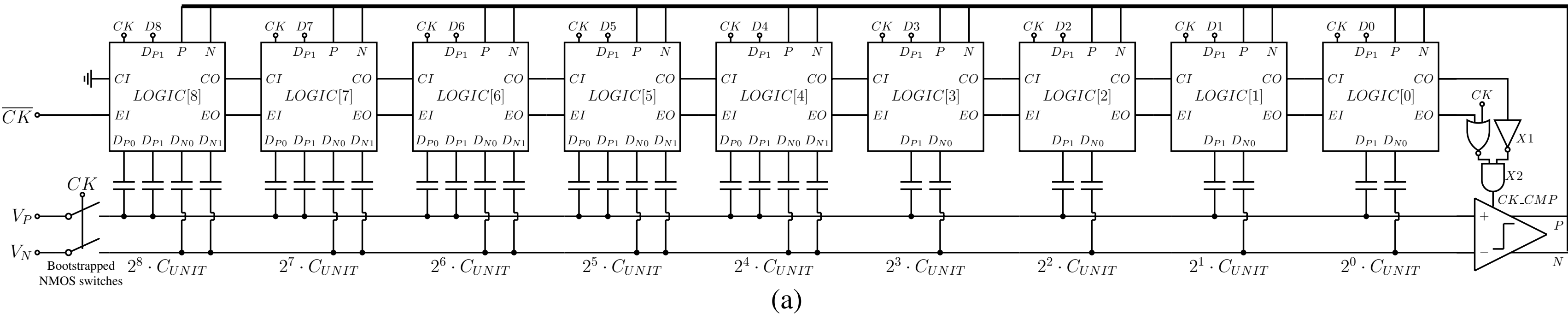
Abstract—This paper presents a low-power 9-bit compiled successive-approximation register (SAR) analog-to-digital converter (ADC) for Bluetooth low energy receivers. The ADC is compiled from a SPICE netlist, a technology rule file, and an object definition file into a design rule check and layout versus schematic clean layout and schematic in 28-nm FDSOI. The compiled SAR ADC reduces the design time necessary to port to a new technology, and to demonstrate technology porting the same SAR ADC architecture is compiled in 28-nm FDSOI with Input/Output (IO) transistors. This paper also includes a comparator clock generation loop that uses the bottom plate of the capacitive digital-to-analog converter. The proposed compiled core transistor SAR ADC achieves the state-of-the-art Figure of Merit (FoM) of 2.7 fJ/conv.step at 2 MS/s, and 3.5 fJ/conv.step at 20 MS/s with an area of 0.00312 mm².

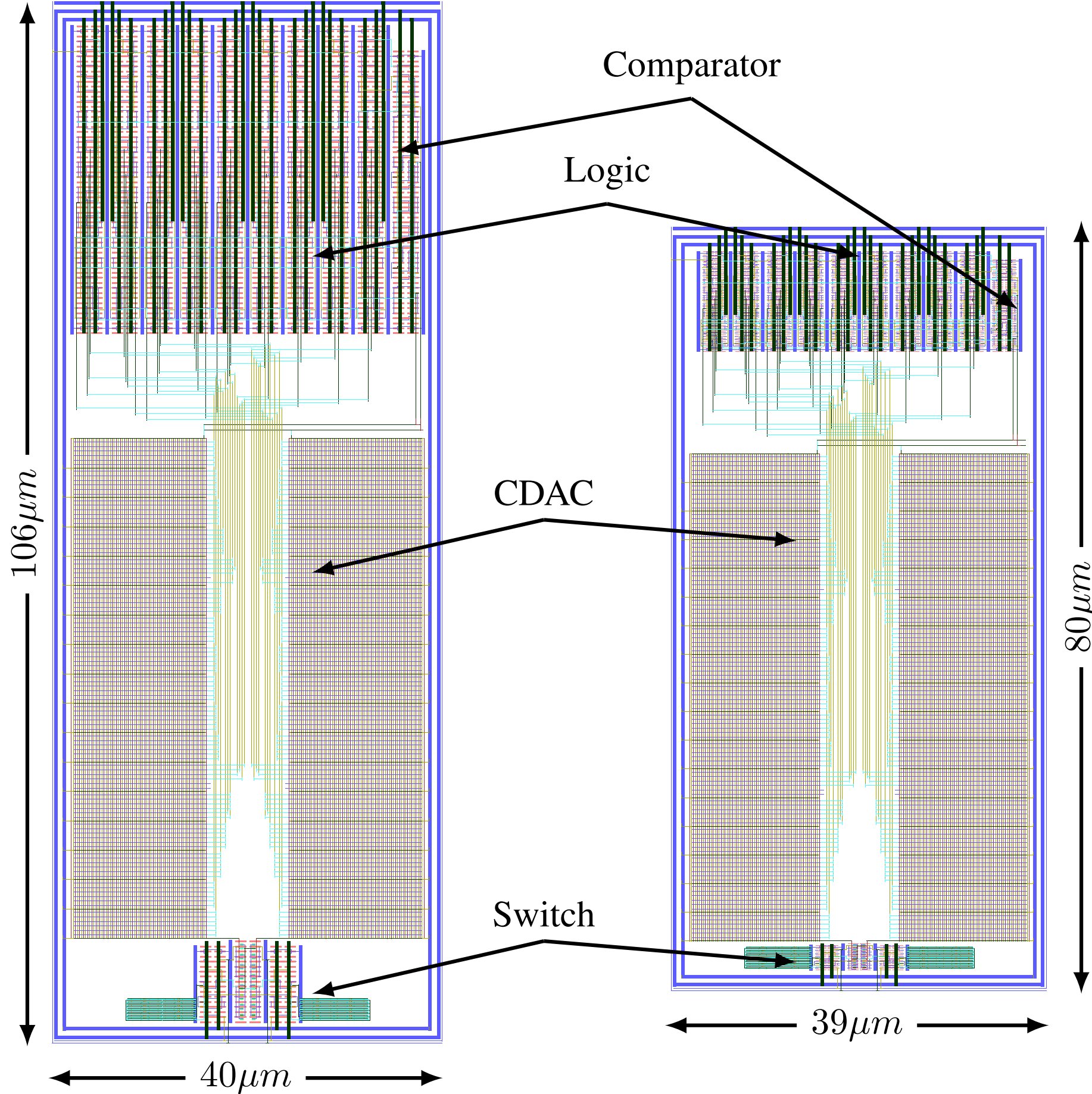
Index Terms—Analog layout, analog layout synthesis, analog-to-digital conversion, analog-to-digital converter (ADC), Bluetooth low energy, Fully-depleted Silicon-on-insulator (FDSOI), low power, successive approximation.

layout. For example, the schematic does not contain placement information for layout, since the optimum layout placement might be different from optimal schematic placement.

Analog layout generation has a long history with works from the previous century [2], [3], but the state-of-the-art analog layout generation, as reviewed in [4], is not widely adopted. More promising research avenues avoid the challenge of analog layout generation from schematics, by not having a schematic. Recently, ADCs have been compiled in a digital flow [5], [6], and although the Effective Number of Bits (ENOB) was less than 6 bit, it is an interesting approach. A similar approach has been used successfully for all-digital Phase Locked Loops [7].

This paper, first introduced at a conference [8], presents a method where the layout is not generated based on drawn schematics. The ADC is described using an approach borrowed from object oriented programming. A custom compiler





(a)

(b)

A 68 dB SNDR Compiled Noise-Shaping SAR ADC With On-Chip CDAC Calibration

Harald Garvik, Carsten Wulff and Trond Ytterdal

Department of Electronic Systems

Norwegian University of Science and Technology (NTNU), Trondheim, Norway

Email: harald.garvik@ntnu.no

Abstract—This paper presents a noise-shaping SAR ADC with an on-chip, foreground capacitive DAC calibration system. At start-up, the ADC uses the smallest DAC capacitors to measure and digitize the errors of the largest ones. A synthesized digital module accumulates the noise-shaped measurements, computes calibration coefficients, and corrects ADC codes at run-time. The loop filter implements two optimal zeros and two poles, and achieves 27.8 dB in-band attenuation at an oversampling rate of 4. The prototype implemented in 28 nm FDSOI achieves 68.2 dB SNDR at 5 MHz bandwidth while using 108.7 μW . The Walden figure-of-merit is 5.2 fJ/conv.-step. The layout of the ADC is compiled from a netlist, a rule file, and an object definition file.

Index Terms—Noise-shaping, SAR ADC, CDAC calibration, analog layout synthesis.

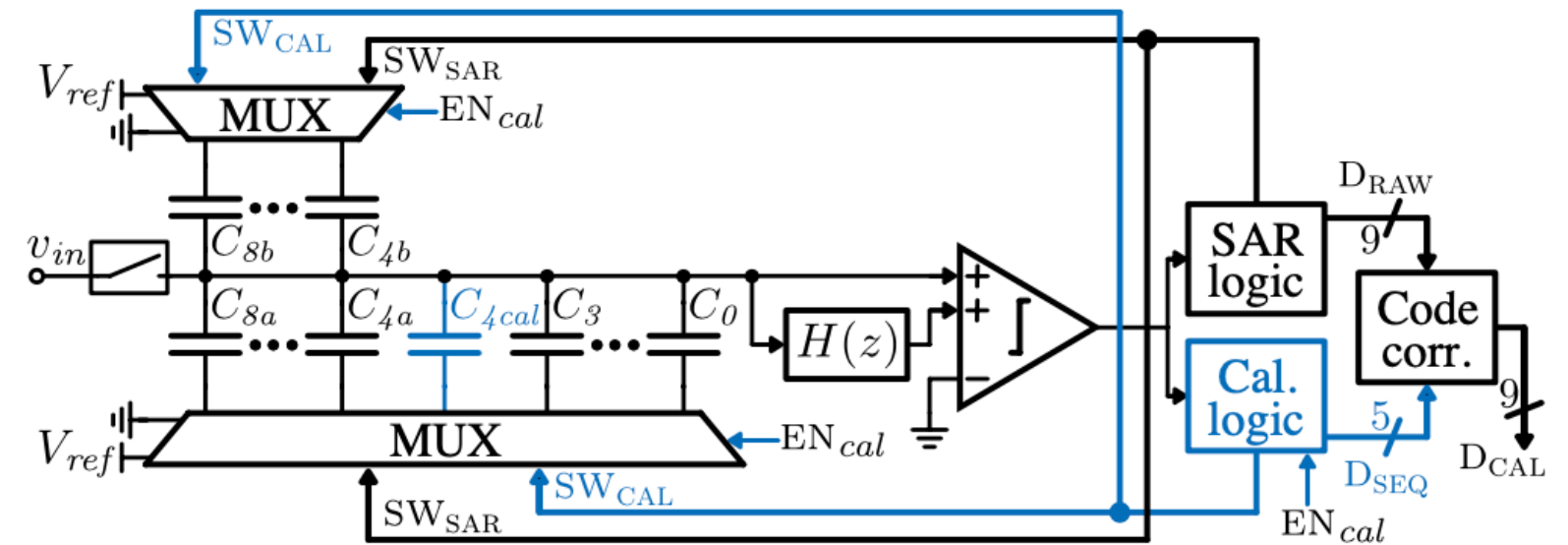


Fig. 1. Proposed noise-shaping SAR architecture. Blue blocks and paths are only active in calibration mode.

AD-PLLL

Phase Locked loops

- Read Razavi's PLL book ⁷

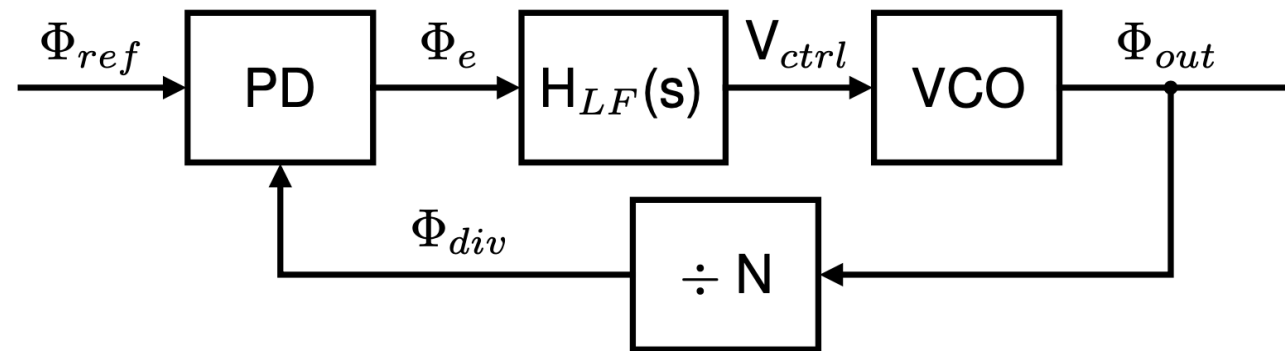
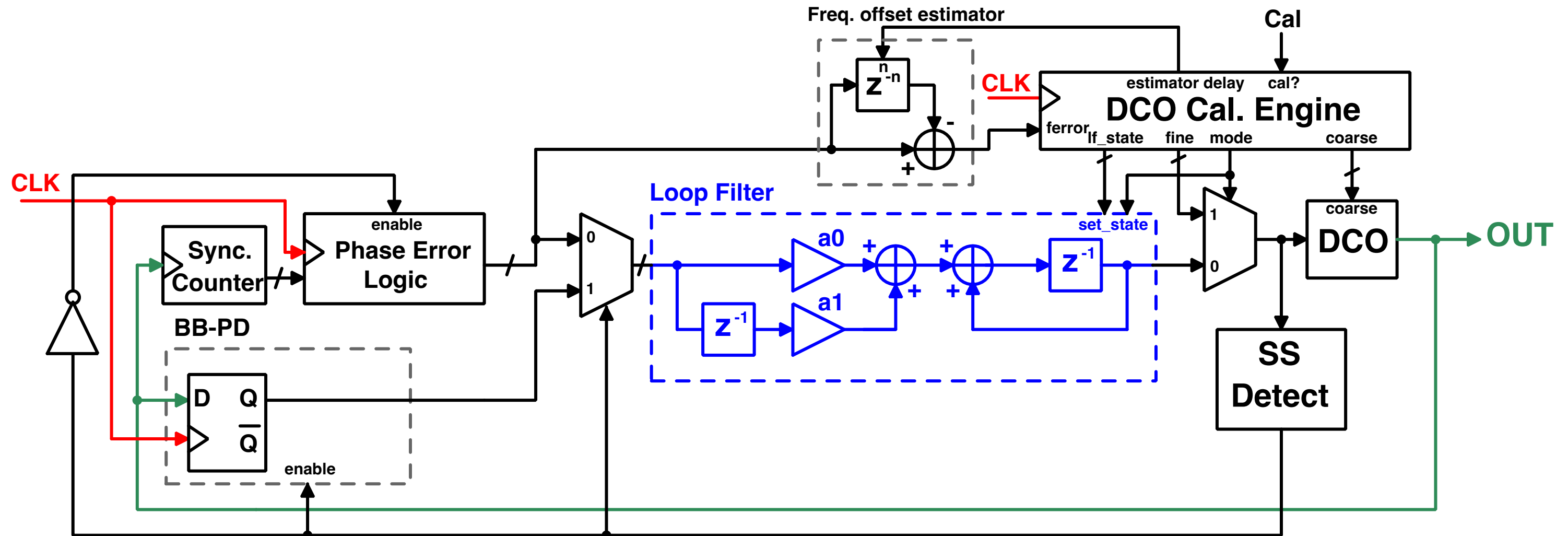


Figure 2: Basic PLL.

⁷ Design of CMOS Phase-Locked Loops, Behzad Razavi, University of California, Los Angeles

AD-PLL with Bang-Bang phase detector for steady-state ⁵



⁵ Cole Nielsen, https://github.com/nielscol/thesis_presentations

Baseband

Baseband block

Why

Mixer?

If we're using low intermediate frequency to avoid DC offset problems and flicker noise

Channel filters?

If the AAF is insufficient for adjacent channel

Power detection

To be able to control the gain of the radio

Phase extraction

Assuming we're using FSK

Timing recovery

Figure out when to slice the symbol

Bit detection

single slice, multi-bit slice, correlators etc, see

Address detection

Is the packet for us?

Header detection

What does the packet contain

CRC

Does the packet have bit errors

Payload decrypt

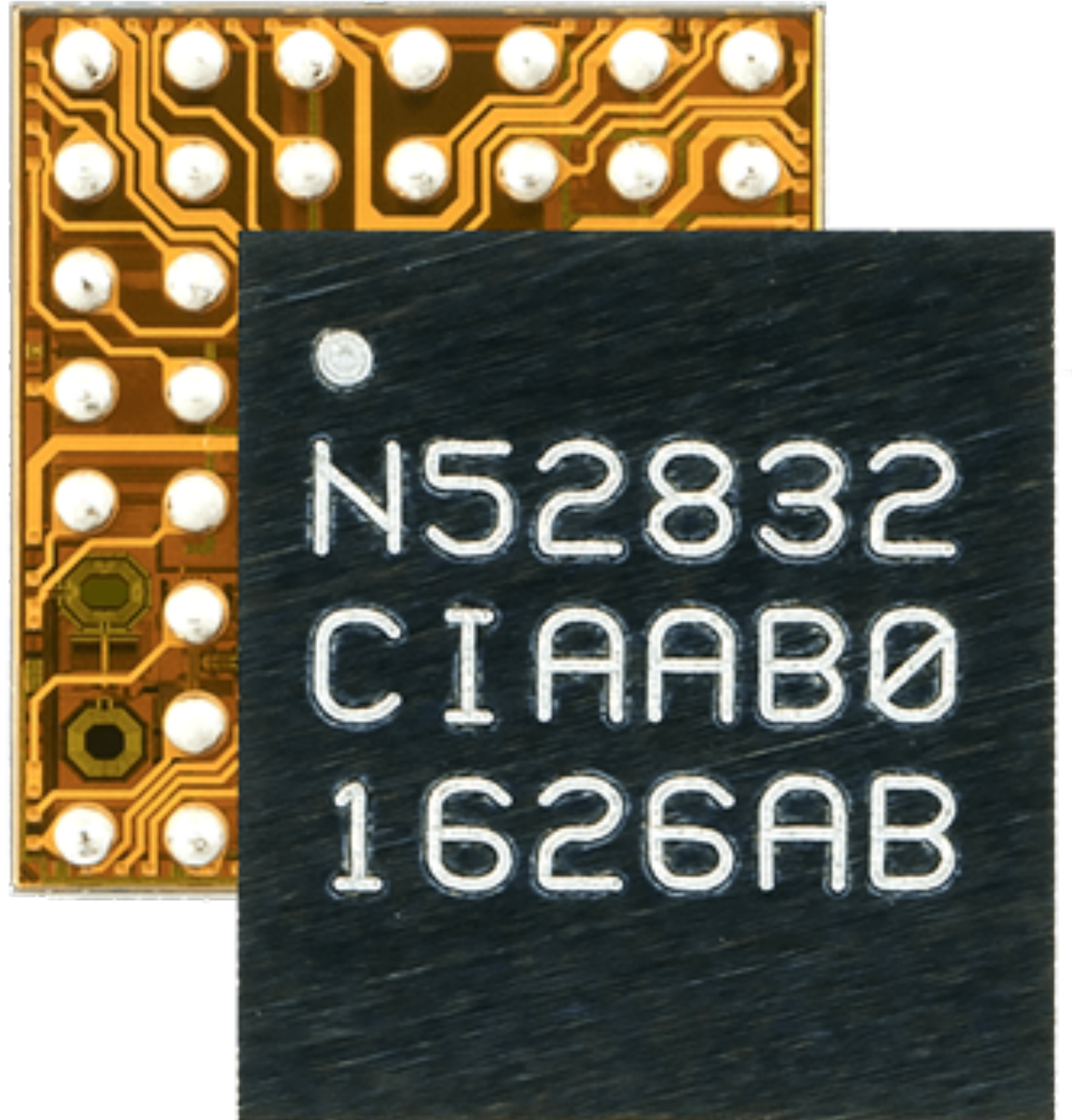
Most links are encrypted by AES

Memory access

Payload need to be stored until CPU can do something

What do we really want,
in the end?

$$P_{RX_{sens}} = -174 \text{ dBm} + 10 \log_{10}(DR) + NF + Eb/N0$$



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