TFE4188 - Introduction to Lecture 7

Voltage regulation

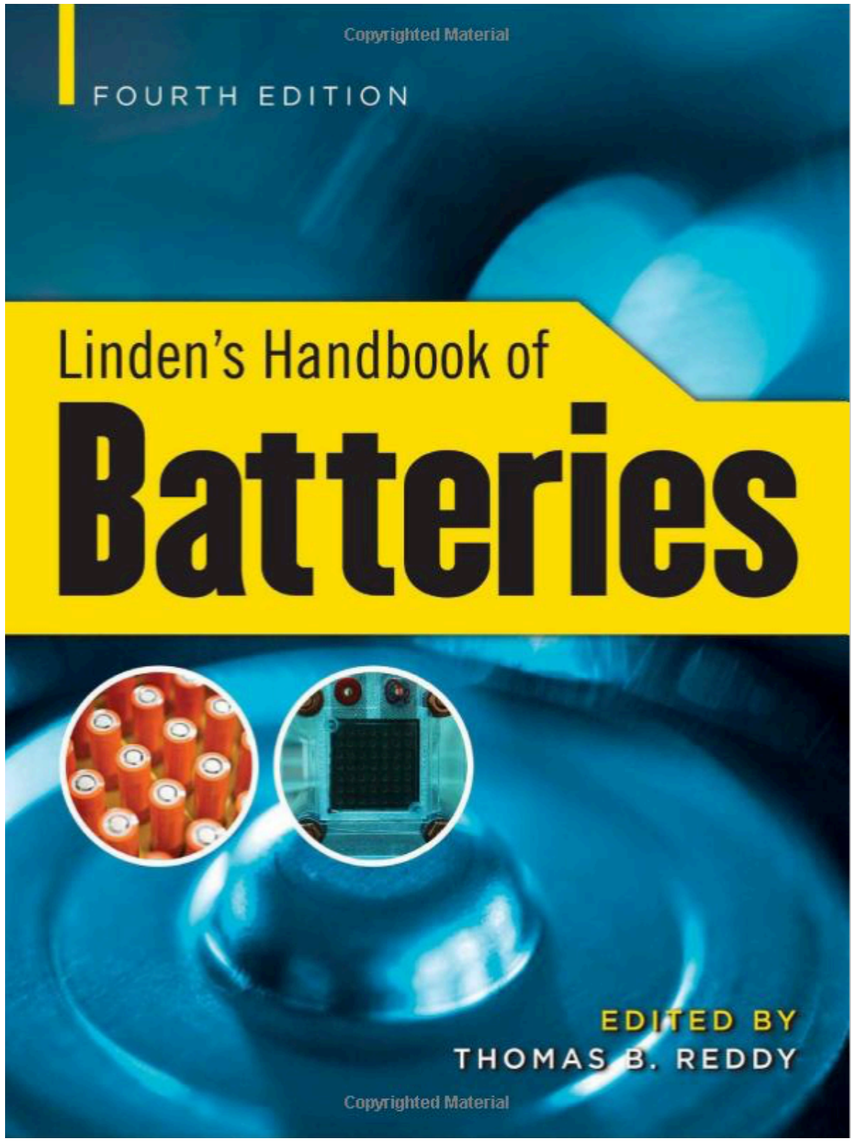
Goal

Why do we need voltage regulation

Introduction to **linear regulators**

Introduction to **switched regulators**

Why



Voltage source

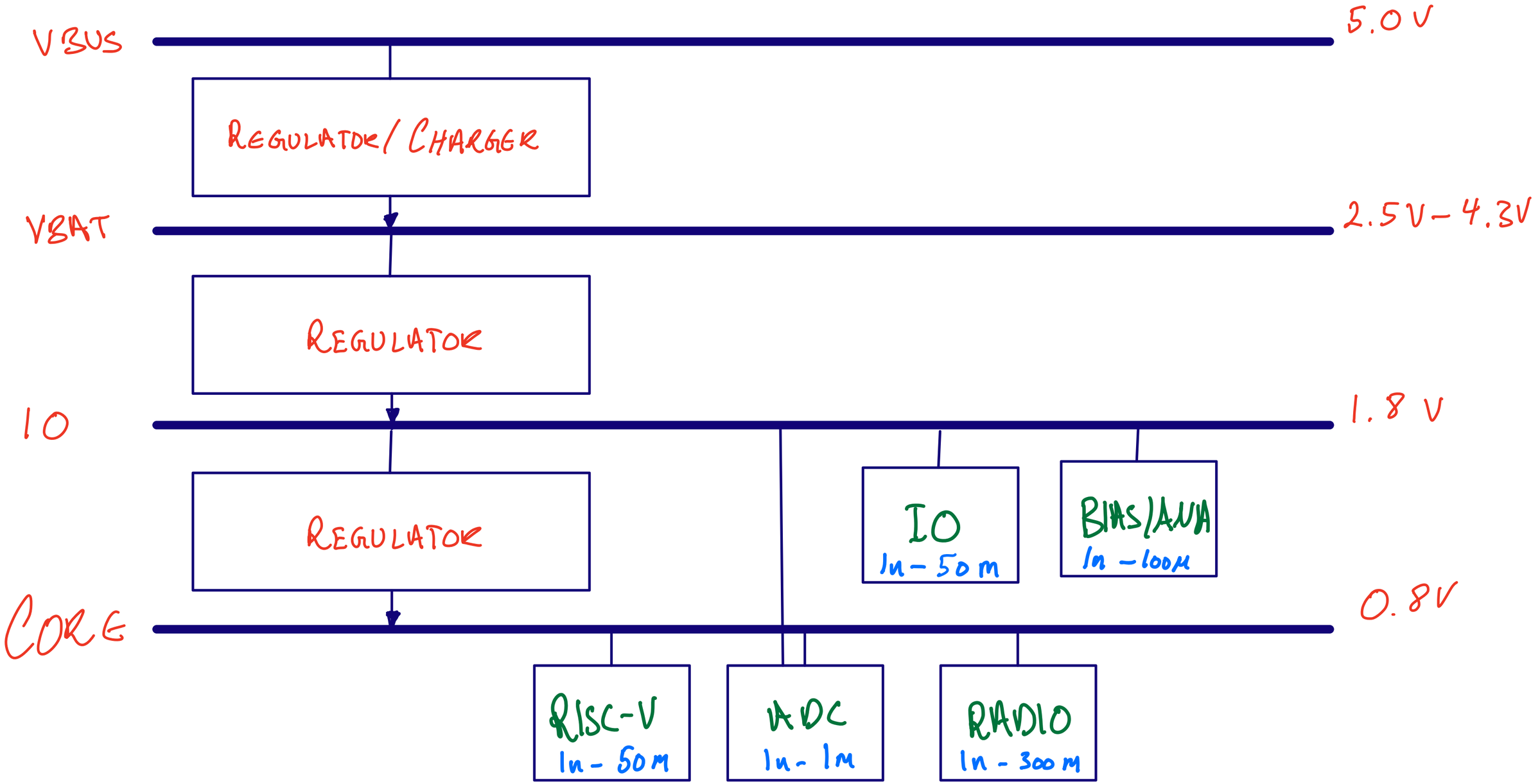
	Chemistry	**Voltage [V]**
Primary Cell	LiFeS2 + Zn/ Alk/MnO2 + LiMnO2	0.8 - 3.6
Secondary Cell	Li-Ion	2.5 - 4.3
USB	-	4.0 - 6.5 (20)

Core

Node [nm]	**Voltage [V]**
180	1.8
130	1.5
55	1.2
22	0.8

IO

Voltage [V]
5.0
3.0
1.8
1.2


VBUS
5.0 V
REGULATOR / CHARGER
VBAT
2.5V - 4.3V
REGULATOR
IO
1.8 V
REGULATOR
IO
In - 50 m
BIAS/ANA
In - 100µ
CORE
0.8V
RISC-V
In - 50 m
ADC
In - 1m
RADIO
In - 300 m

Name	Voltage	Min [nA]	Max [mA]	PWR DR [dB]
VDD_VBUS	5	10	500	77
VDD_VBAT	4	10	400	76
VDD_IO	1.8	10	50	67
VDD_CORE	0.8	10	350	75

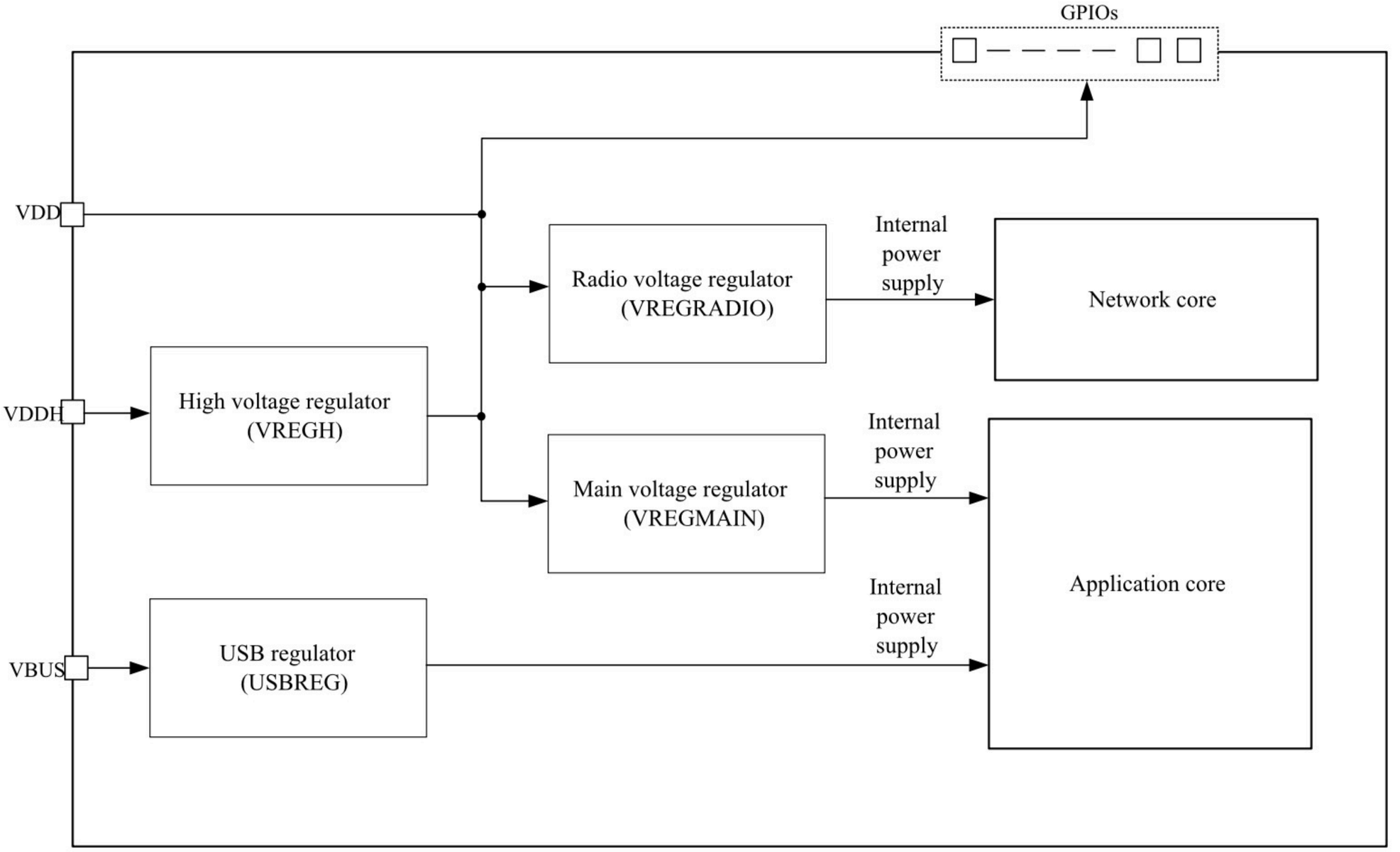
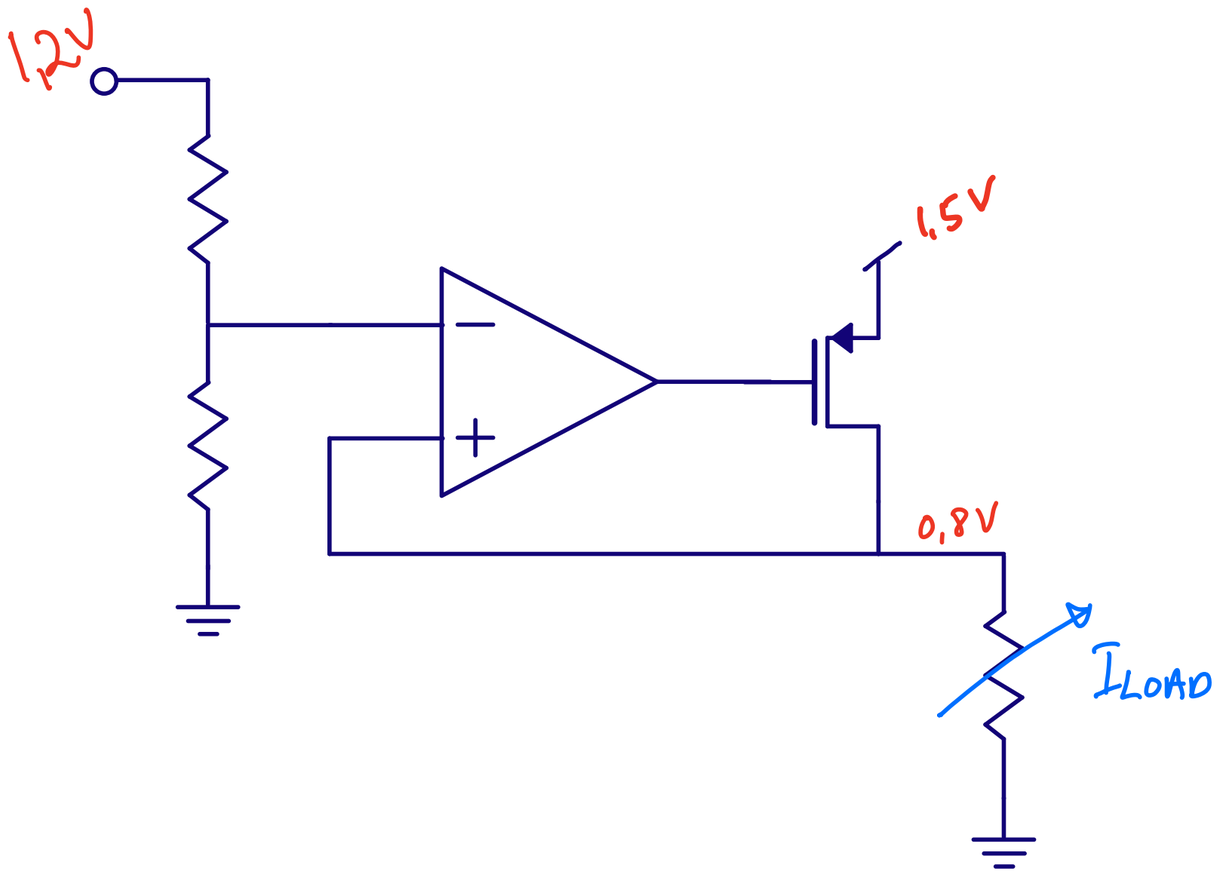


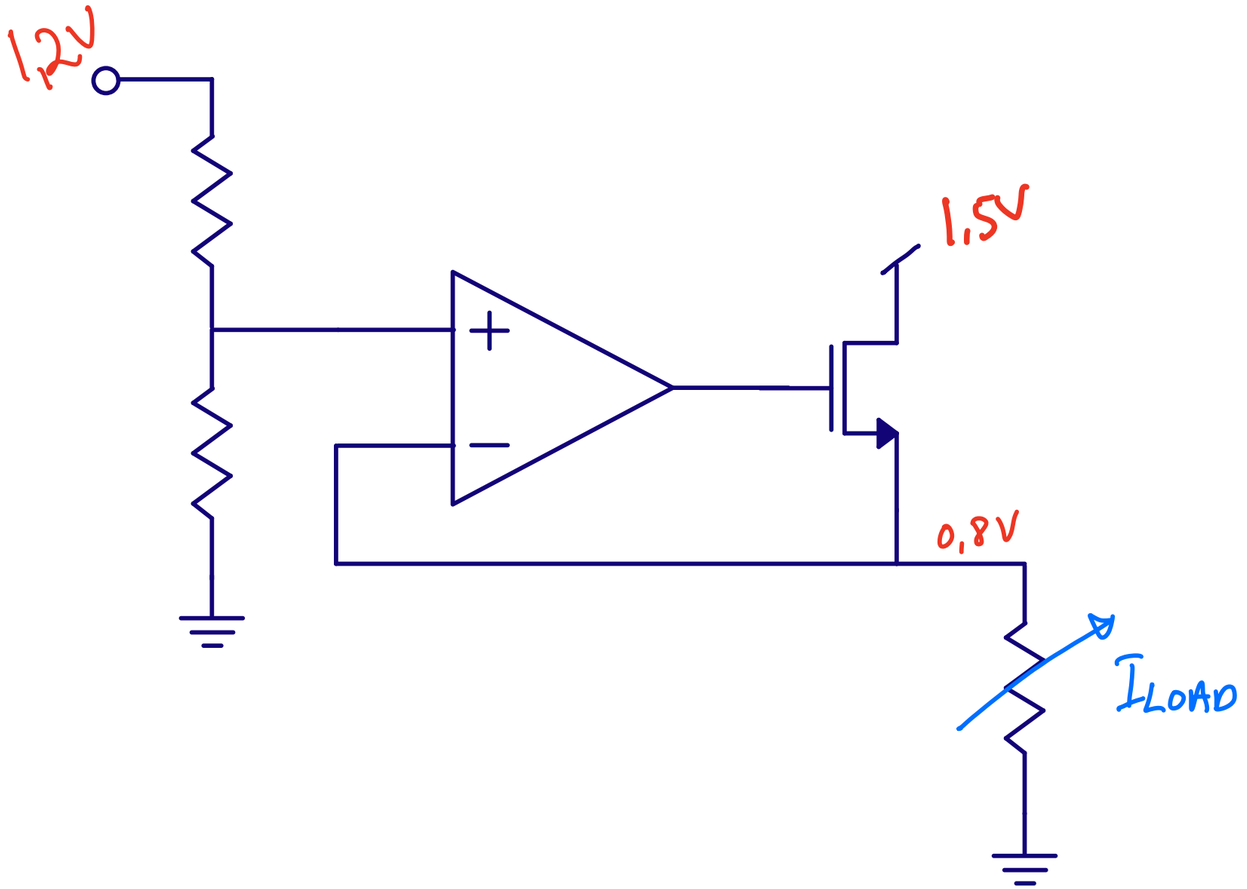
Figure 1. Regulators used in nRF5340

Linear Regulators



PMOS pass fet

NMOS pass fet



LDO's in JSSC

IEEE JOURNAL OF SOLID-STATE CIRCUITS 1

A Scalable High-Current High-Accuracy Dual-Loop Four-Phase Switching LDO for Microprocessors

Xiangyu Mao, Yan Lu, *Senior Member, IEEE*, and Rui P. Martins, *Fellow, IEEE*

***Abstract*— High-performance microprocessors need high current (ampere-level), high accuracy, and fast-response power supplies. Comparing to analog and digital low-dropout (LDO) regulators, the switching LDO can be a better candidate for such requirements, as it can drive large power transistor(s) fast and accurately. However, conventional switching LDOs need large load capacitance to reduce the output ripple, which restricts their applications. This article presents a 1.5-A fully-integrated switching LDO for microprocessors, with an easily scalable load capability. Here, we introduce three techniques together to relief**

since the highest frequency core dictates the minimum V_{IN} level, other low-frequency cores will waste extra power. Fully-integrated voltage regulator can supply the local voltage domain for per-core dynamic voltage and frequency scaling (DVFS), as shown in Fig. 1 [1].

Inductor-based converters usually offer high efficiency with a high-quality factor (Q) power inductor. However, implementing high-Q inductors on silicon is challenging. In [2], buck converters have been demonstrated using on-chip induc-

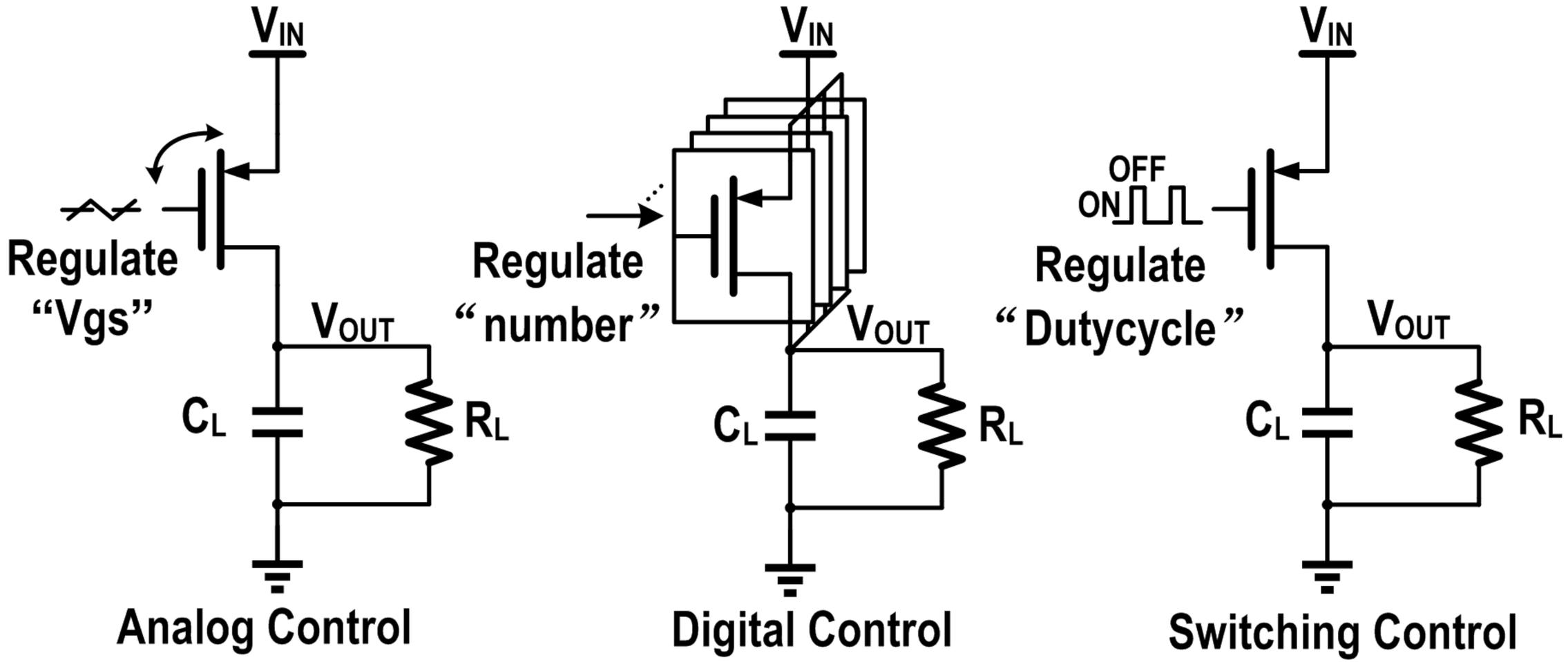
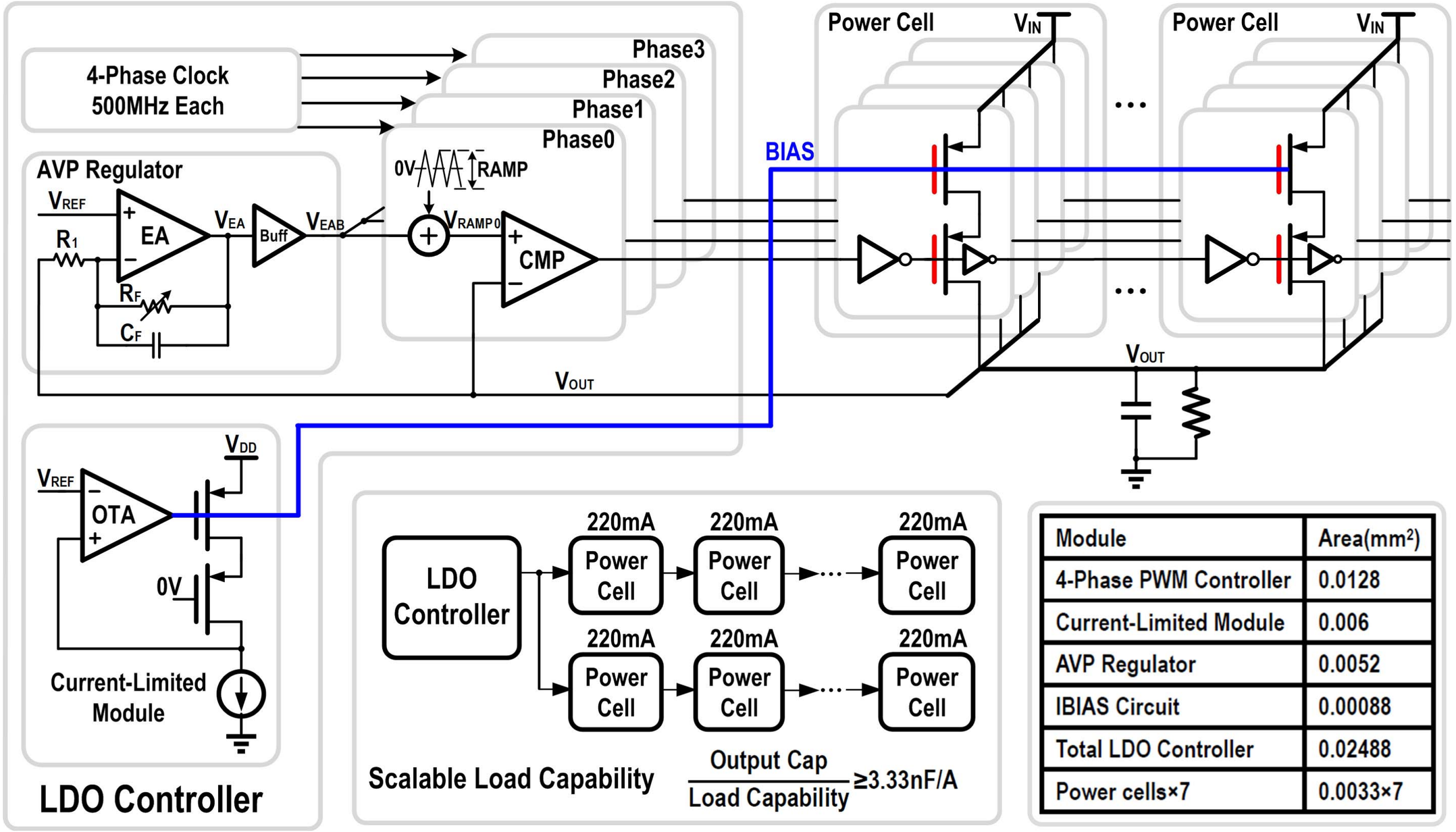


Fig. 2. LDO control methods.



Module	Area(mm^2)
4-Phase PWM Controller	0.0128
Current-Limited Module	0.006
AVP Regulator	0.0052
IBIAS Circuit	0.00088
Total LDO Controller	0.02488
Power cells×7	0.0033×7

Fig. 17. System architecture of the proposed LDO with scalable load capability.

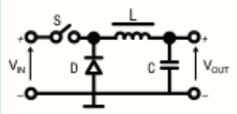
Switched Regulators

Reference Guide to Switched DC/DC Conversion

DC/DC converters convert one DC voltage level to another. Switched-mode DC/DC converters use a FET switch and a storage element to first store energy, then release it to achieve the desired output voltage. The common arrangements of switches and storage elements, or topologies, are shown below.

Non-isolated, non-inverting topologies, output voltage at same polarity as input.

Step-down or Buck converter

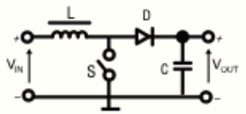


$0 \le V_{OUT} \le V_{IN}$ $V_{OUT} = d*V_{IN}$

Simple step down circuit with single switch (FET) and storage element (inductor). The output capacitor C is needed to remove significant output ripple. Synchronous version replaces D with second FET.

Ref: https://www.mouser.com/applications/power-supply-topology-buck/

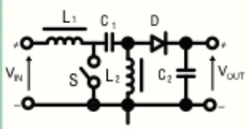
Step-up or Boost converter



$V_{OUT} \ge V_{IN}$ $V_{OUT} = V_{IN}/(1-d)$

Simple step up circuit with single switch and storage element. The output capacitor C is needed to remove significant output ripple. Synchronous version replaces D with second FET

SEPIC (Single-ended primary-inductor converter)

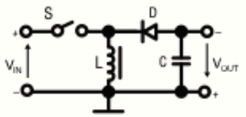


$V_{OUT} = d*V_{IN}/(1-d)$

Can step-up or step down as required to maintain a fixed output voltage. Vout is fixed by the switching duty cycle. Can use coupled inductors to save PCB space.

Non-isolated, inverting topologies – output voltage polarity reversed vs input

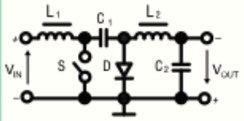
Inverting (buck-boost)



$V_{OUT} = -d*V_{IN}/(1-d)$

Simple single switch and inductor topology. Maintains a stable but inverted output voltage, with varying input voltage. The output capacitor C is needed to remove significant output ripple.

Ćuk (Pronounced 'Chook')



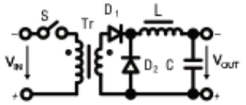
$V_{OUT} = -d*V_{IN}/(1-d)$

A buck-dboost topology with inverted output voltage and very low ripple current. Can use coupled inductors to save PCB space. Ideal for applications needing stable smooth output from varying input source.

Note: The output current is continuous and ripple-free

Isolated Topologies

Forward converter

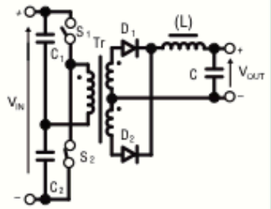


$V_{OUT} = V_{IN}*d*(Ns/Np)$

Can provide Vout higher or lower than Vin and electrical isolation via a transformer. Higher output power (generally up to 200W) along with higher energy efficiency than Flyback topology.

Ref: https://www.mouser.com/applications/power-supply-topology-forward/

Push-pull (Half Bridge)

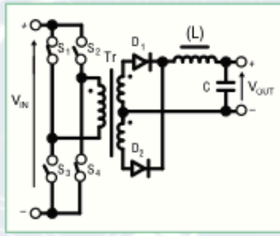


$V_{OUT} = 2*V_{IN}*d*(Ns/Np)$

Can provide Vout higher or lower than Vin, gives electrical isolation via a transformer, output power up to 500W along with higher energy efficiency than Flyback topology.

https://www.mouser.com/applications/power-supply-topology-half/

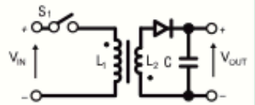
Full bridge



$V_{OUT} = 2*V_{IN}*d*(Ns/Np)$

A robust buck converter topology, similar to half-bridge, can provide Vout higher or lower than Vin. Often used in higher power applications such as EV charging and renewable energy systems.

Flyback



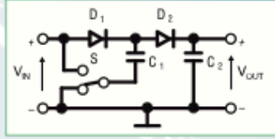
$V_{OUT} = V_{IN}/(1-d)$

Simple single transistor topology, typically used for offline, low output power (<100W) applications such as cellphone chargers. Fixed Vout determined by transformer.

Ref: https://www.mouser.com/applications/power-supply-topology-flyback/

Charge Pumps DC/DC converters that use capacitors as the storage element are known as Charge Pumps. Suitable for low-power applications, they are typically used to boost or invert input voltage. They may be cascaded in order to obtain even-numbered multiples or fractions.

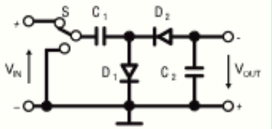
Voltage doubling charge pump



$V_{out} = 2*V_{in} - 2*V_D$

(Where V_D is the voltage drop across the diodes)

Inverting charge pump



$V_{OUT} = -V_{IN} + 2*V_D$

(Where V_D is the voltage drop across the diodes)

Disclaimer: These diagrams are for reference only and not intended to be implemented as complete working designs. The simplified equations shown are for ideal converters and do not account for losses that may occur within components.

Legend

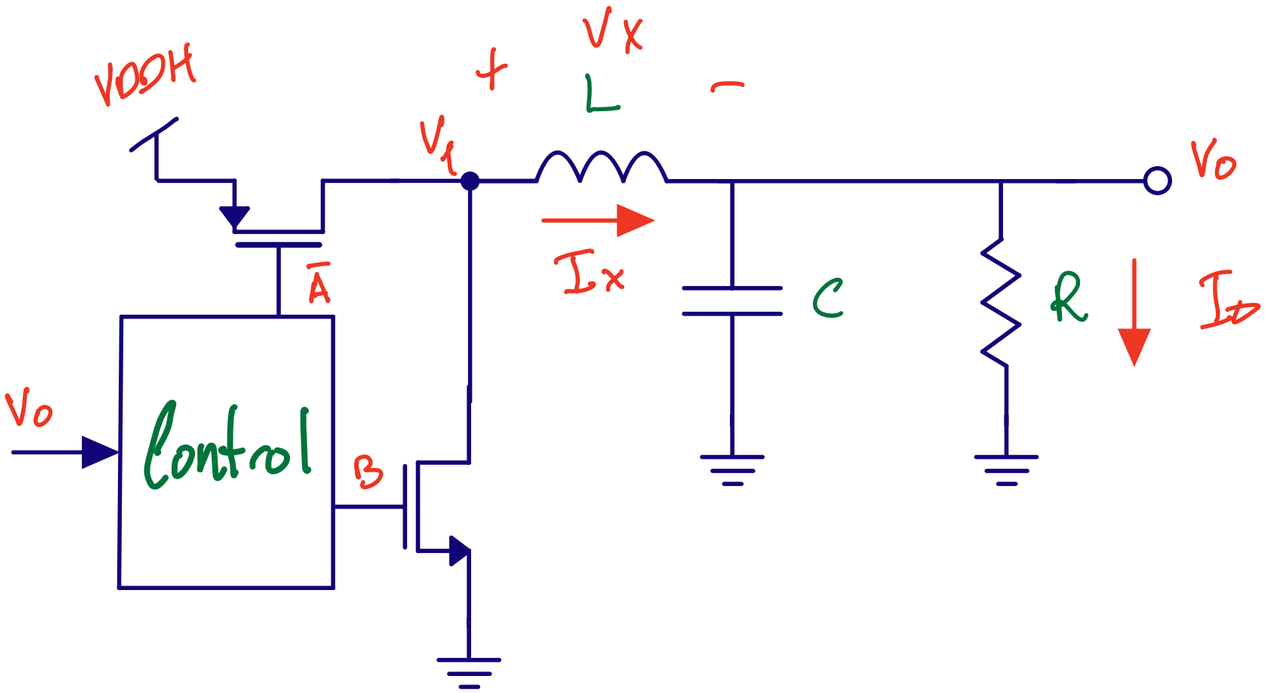
Circuits: D = Diode; C = Capacitor; L = Inductor; Tr = Transformer; V_{IN} = Input voltage; V_{OUT} = Output Voltage

Equations: d = PWM Duty Cycle; Np = Number of turns, primary side; Ns = Number of turns, secondary side

MOUSER ELECTRONICS

Reference Guide to Switched DC/DC Conversion

Inductive DC/DC converters

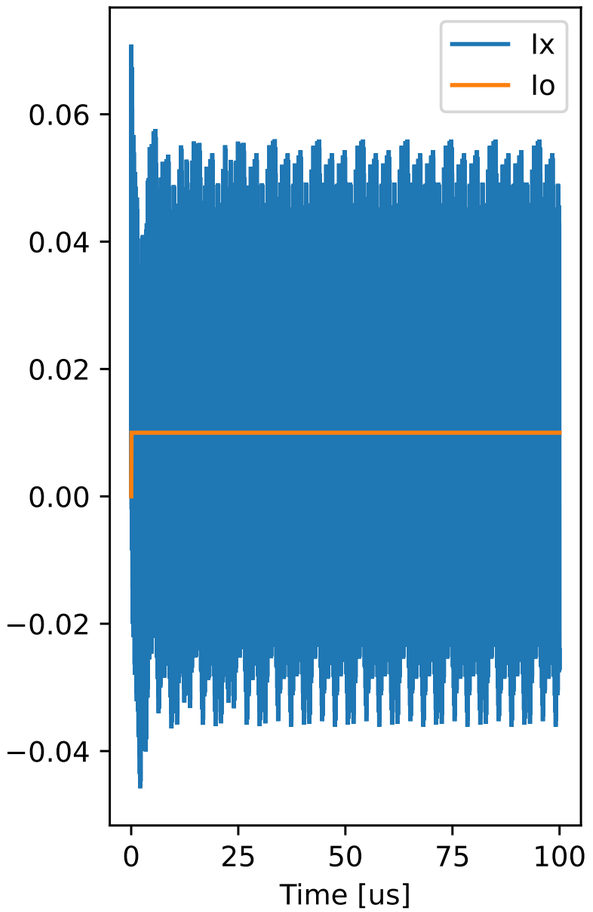


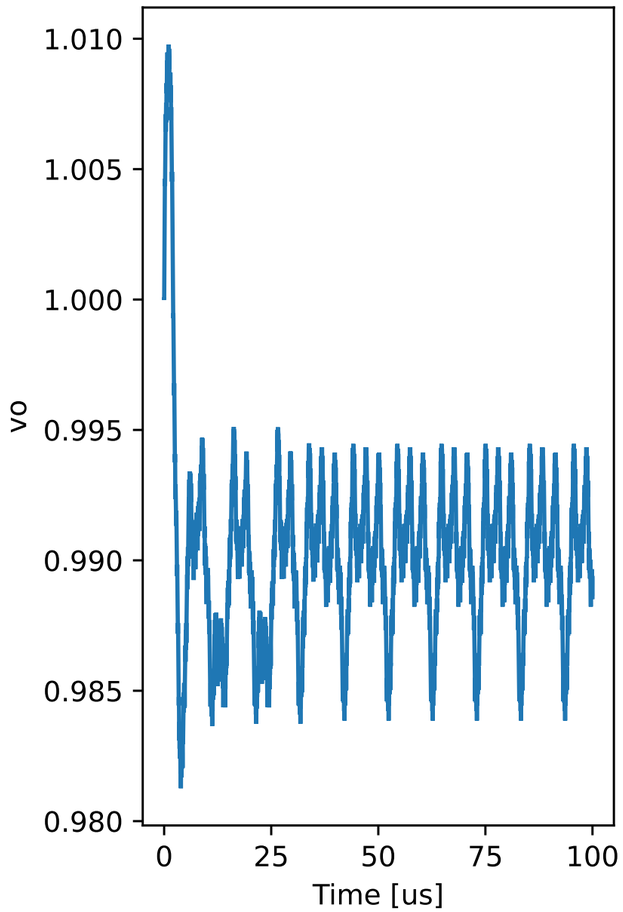
$$I_x(t) = \frac{1}{L}\int V_x(t)dt$$

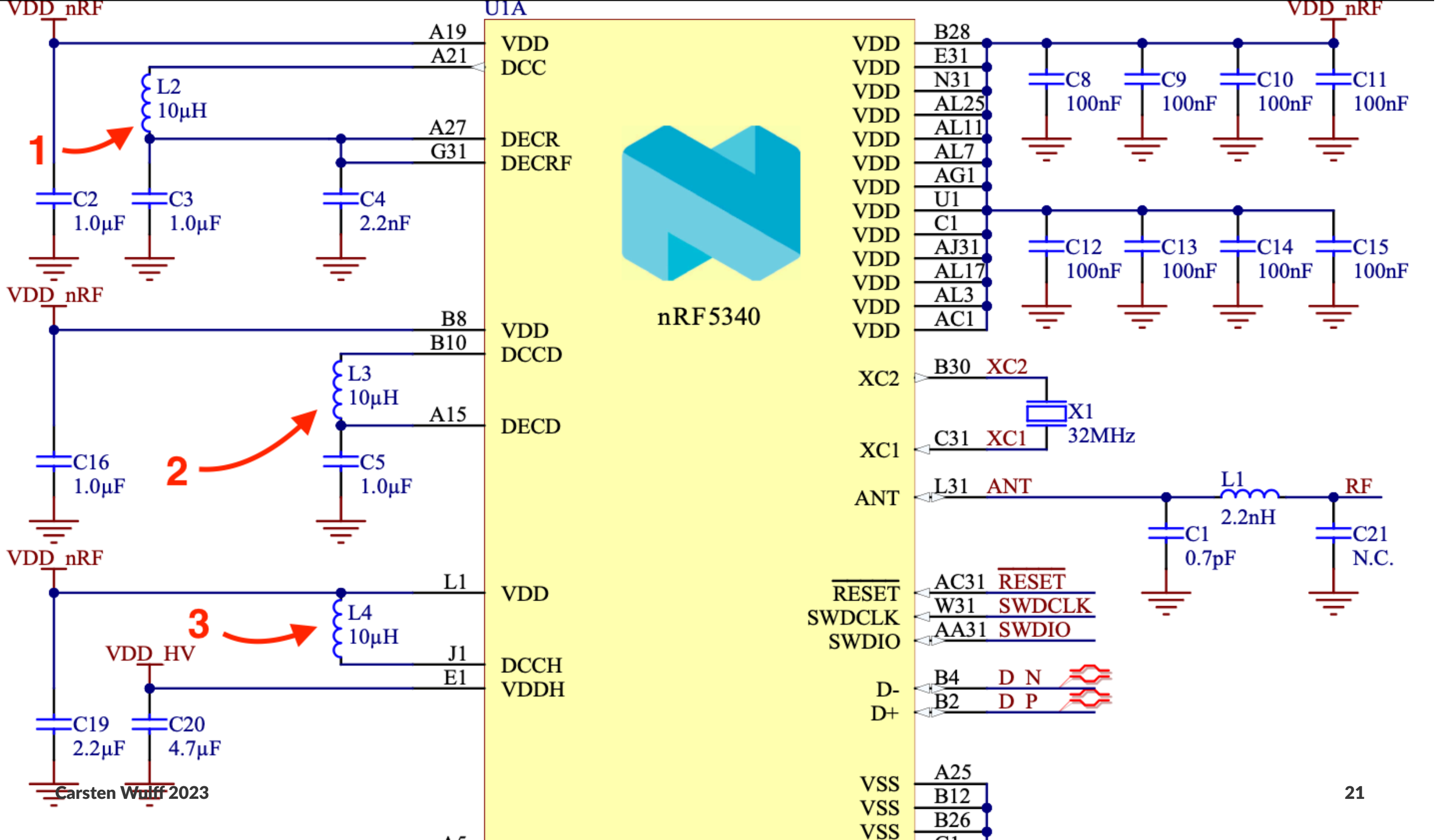
$$V_o(t) = \frac{1}{C}\int (I_x(t) - I_o(t))dt$$

Pulse width modulation (PWM)

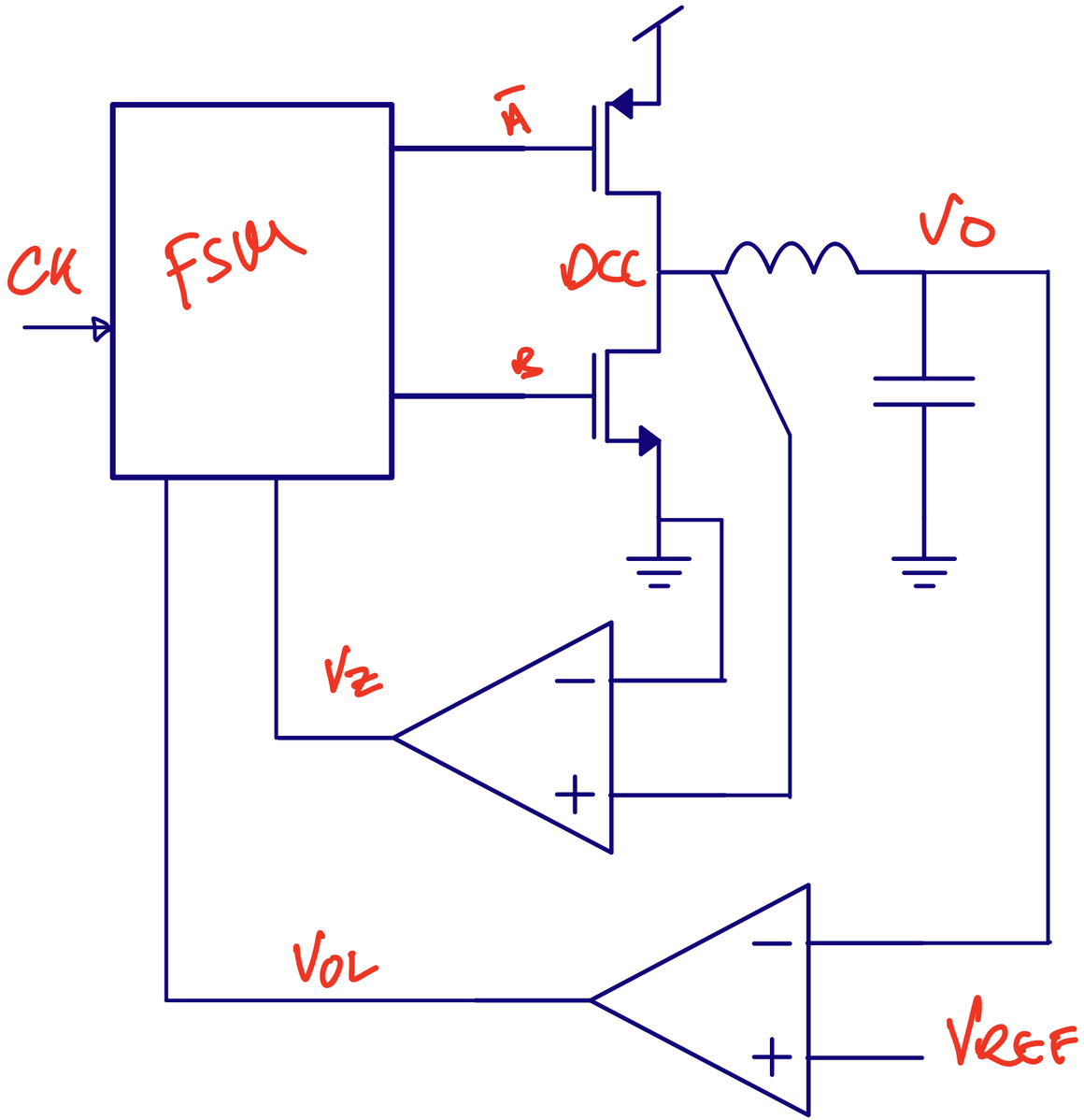
Jupyter PWM BUCK model

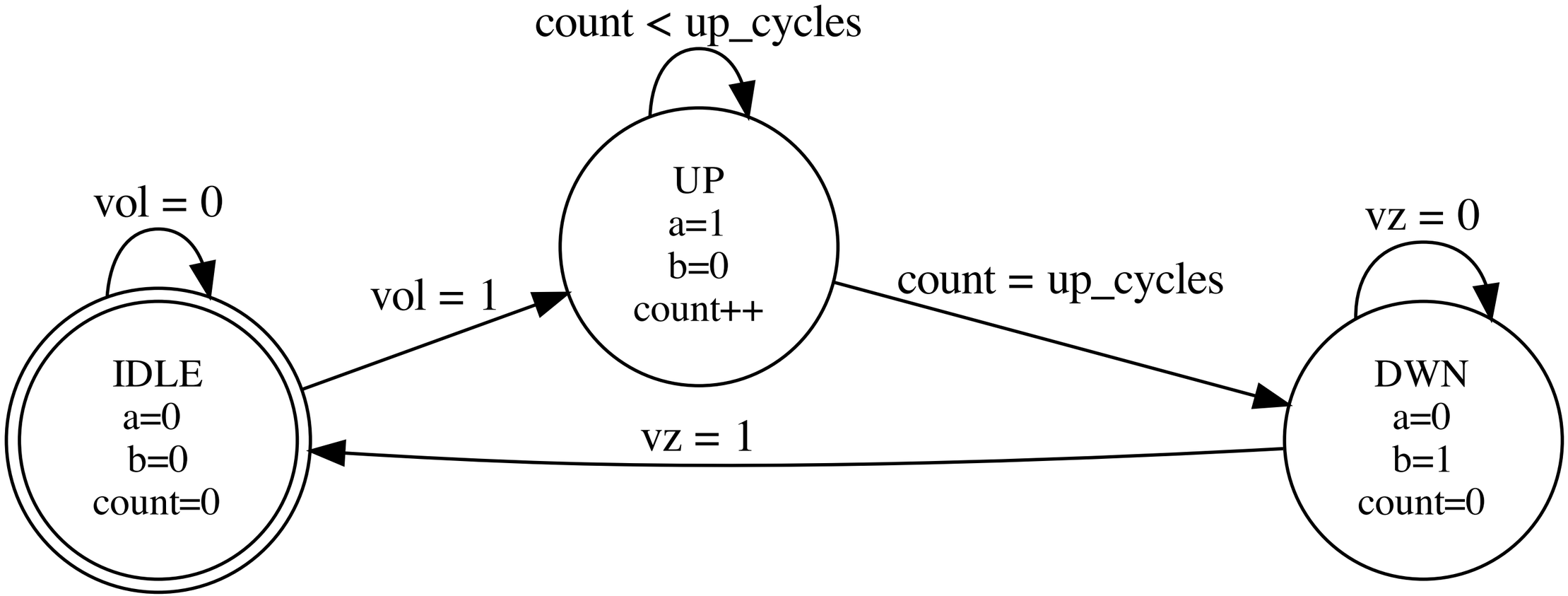




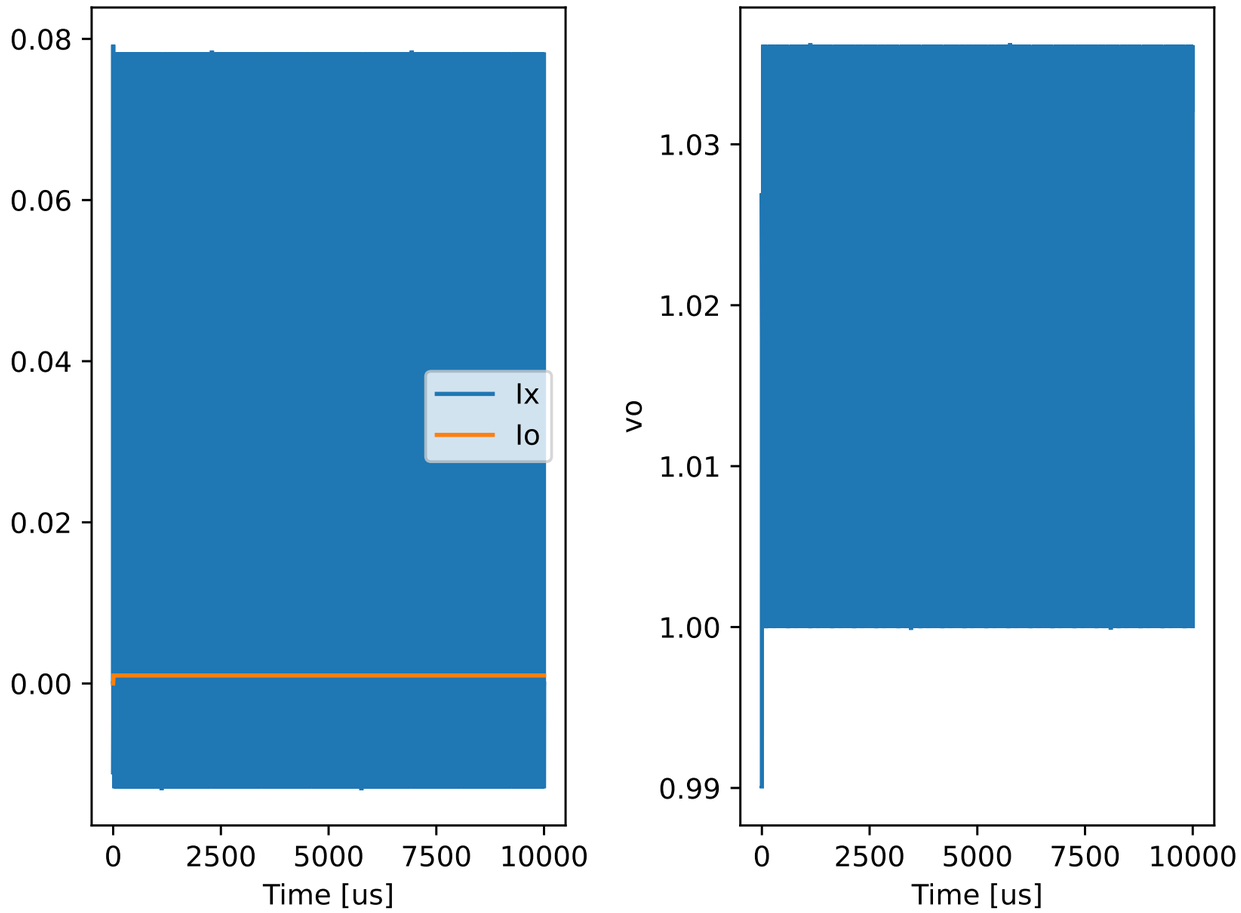

U1A
nRF5340
VDD_nRF
VDD_HV
L2 10µH
L3 10µH
L4 10µH
C2 1.0µF
C3 1.0µF
C4 2.2nF
C16 1.0µF
C5 1.0µF
C19 2.2µF
C20 4.7µF
C8 100nF
C9 100nF
C10 100nF
C11 100nF
C12 100nF
C13 100nF
C14 100nF
C15 100nF
X1 32MHz
L1 2.2nH
C1 0.7pF
C21 N.C.
A19 VDD
A21 DCC
A27 DECR
G31 DECRF
B8 VDD
B10 DCCD
A15 DECD
L1 VDD
J1 DCCH
E1 VDDH
B28 VDD
E31 VDD
N31 VDD
AL25 VDD
AL11 VDD
AL7 VDD
AG1 VDD
U1 VDD
C1 VDD
AJ31 VDD
AL17 VDD
AL3 VDD
AC1 VDD
B30 XC2
C31 XC1
L31 ANT
AC31 RESET
W31 SWDCLK
AA31 SWDIO
B4 D N
B2 D P
A25 VSS
B12 VSS
B26 VSS
1
2
3

Pulsed Frequency Mode (PFM)




count < up_cycles
UP
a=1
b=0
count++
vol = 0
vol = 1
IDLE
a=0
b=0
count=0
count = up_cycles
vz = 0
DWN
a=0
b=1
count=0
vz = 1

Jupyter PFM BUCK model



BUCKs in JSSC

A 10-MHz 2–800-mA 0.5–1.5-V 90% Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes

A 10-MHz 2–800-mA 0.5–1.5-V 90% Peak Efficiency Time-Based Buck Converter With Seamless Transition Between PWM/PFM Modes

Seong Joong Kim, Woo-Seok Choi, Robert Pilawa-Podgurski, and Pavan Kumar Hanumolu, *Member, IEEE*

***Abstract*— Time-based controllers are well suited for implementing both single- and multi-phase wide bandwidth high switching frequency pulsewidth modulation (PWM)-based dc–dc converters. They also consume very little quiescent current but their light load efficiency is severely degraded by switching losses. We explore pulse frequency modulation (PFM) that is commonly used to improve light load efficiency in voltage-mode controllers and extend its operation to time-based controllers. To maintain high efficiency even in the presence of dynamic load variations, we present techniques to perform automatic and seamless switching between PWM/PFM modes. Fabricated in a 65-nm CMOS, the prototype buck converter using the time-based PWM/PFM control achieves 90% peak efficiency and >80% efficiency over a load current range of 2–800 mA. Output voltage changes by less than 40 mV during PWM to PFM transitions.**

***Index Terms*— Buck converter, high switching frequency, light load efficiency, mode switching, pulse frequency modulation (PFM), pulsewidth modulation (PWM), time-based control.**

I. Introduction

the need for a wide bandwidth error amplifier, a pulsewidth modulation (PWM) in analog controllers or a high-resolution analog-to-digital converter (ADC), and a digital PWM in digital controllers. Time-based controller was also shown to be very effective for implementing high-efficiency multi-phase converters [9]. By generating multi-phase control signals with precisely matched duty cycles, a time-based approach achieves implicit passive current matching [9] needed for maximizing efficiency [10], [11]. To summarize, the time-based control enables high F_{SW} compact dc–dc converters that consume low quiescent current and achieve high efficiency over a wide range of load currents through multi-phase operation. However, large switching losses that come with high F_{SW} severely degrade efficiency under light load conditions. Consequently, efficiency of state-of-the-art time-based buck converters deteriorates significantly at light loads (<50 mA) [8], [9]. Because efficiency under light load condition has significant impact on battery

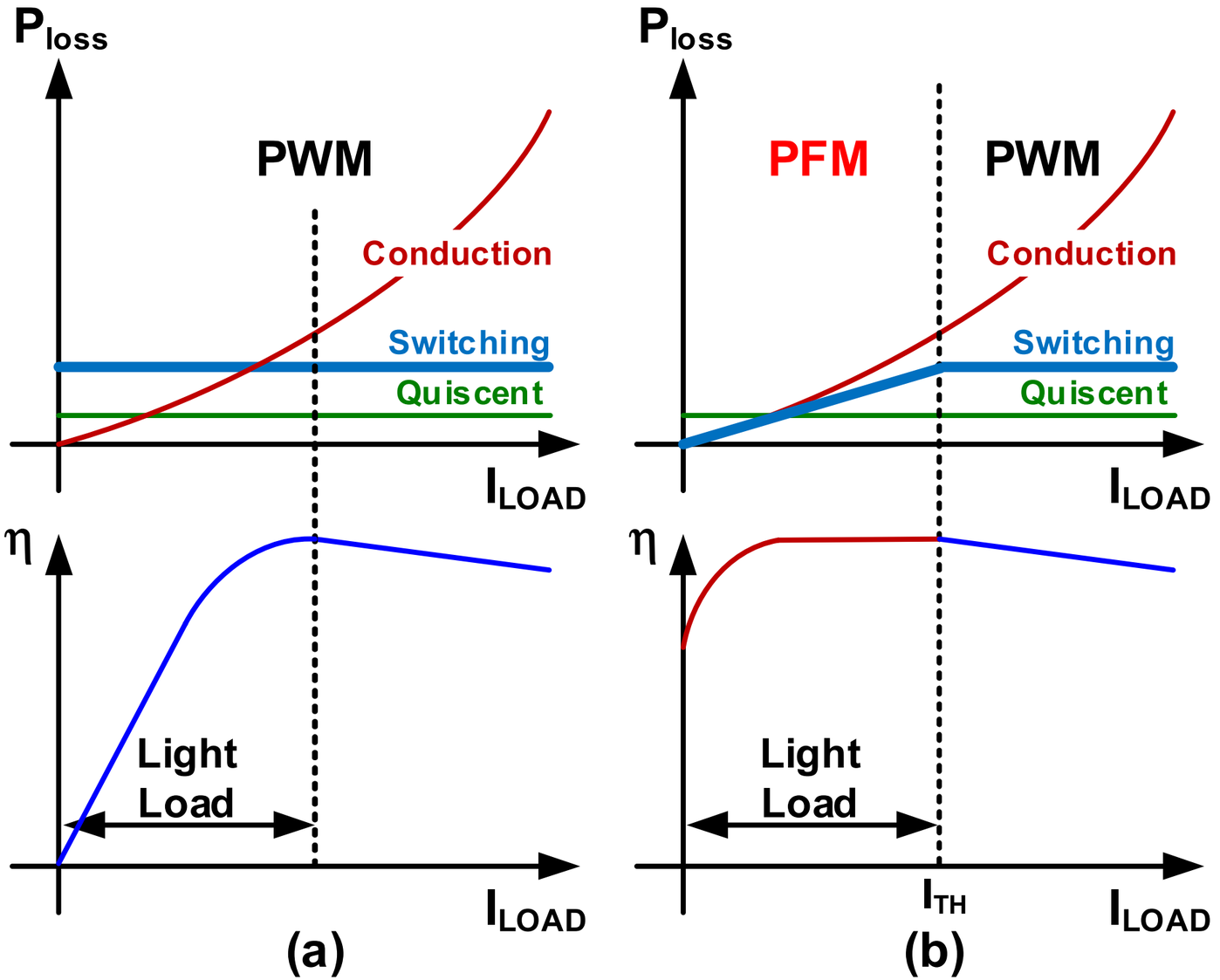


Fig. 1. Loss components and efficiency verses load current in (a) PWM mode and (b) PFM mode.

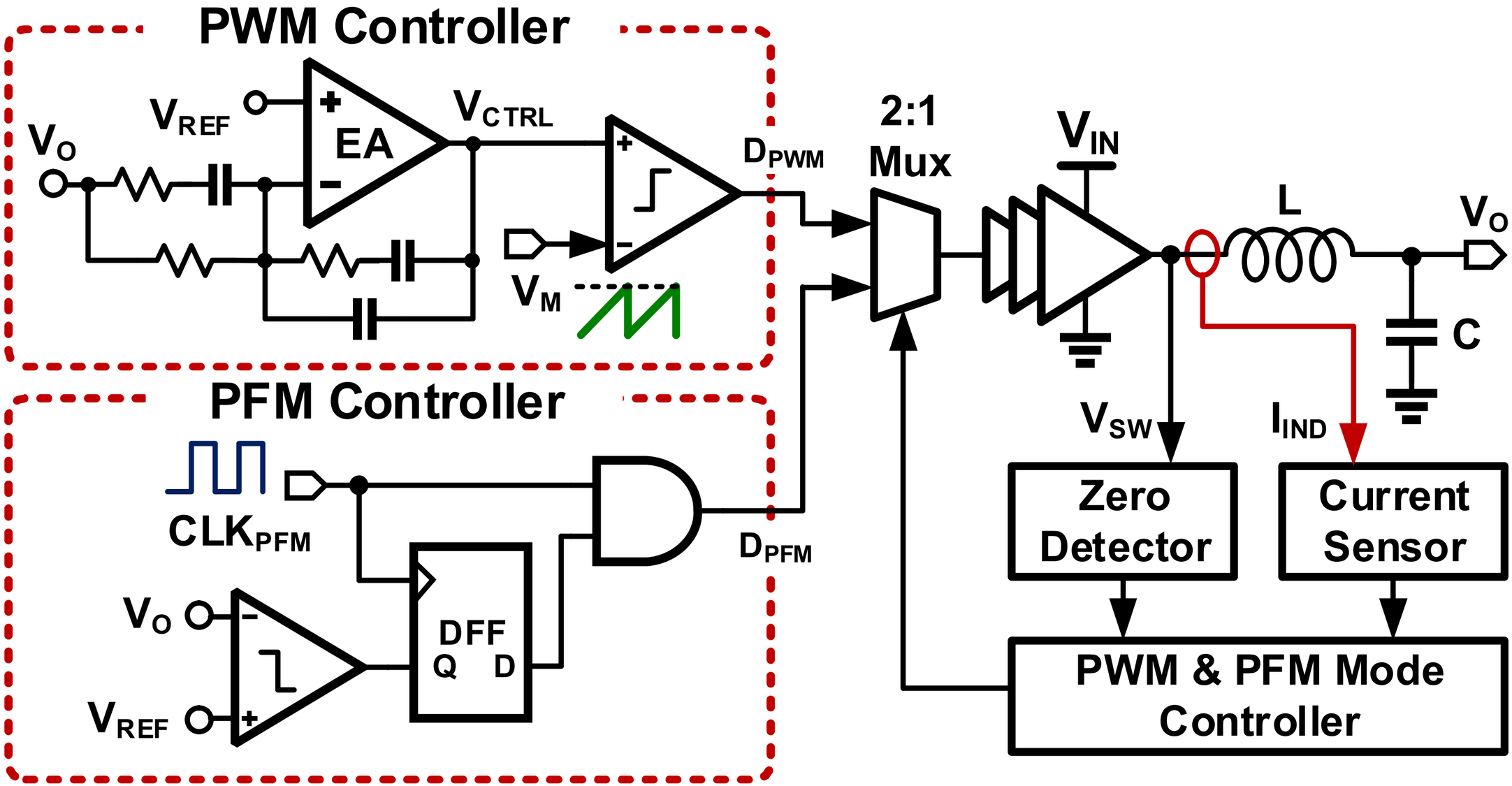
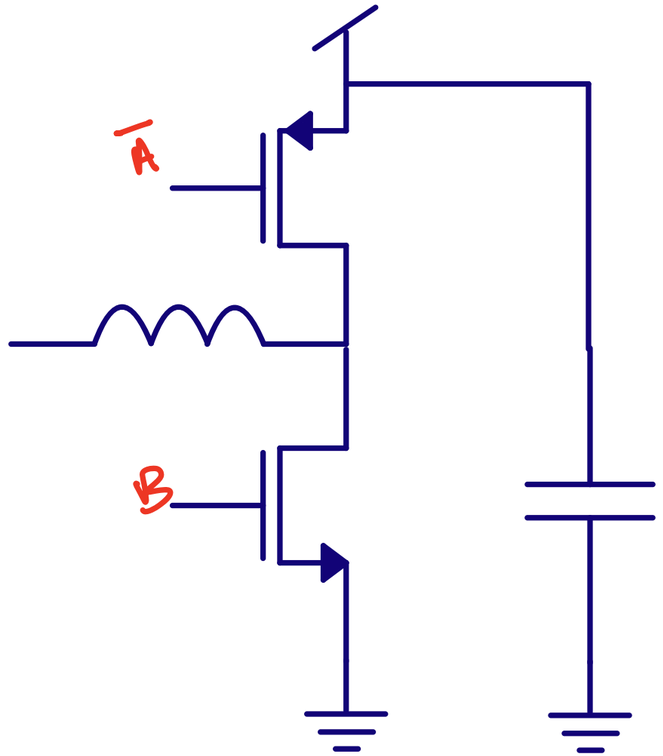


Fig. 7. Simplified buck converter that uses both PWM and PFM modes.

Boost



$$V_O = \frac{V_{in}}{1 - Duty}$$

Thanks!