Integrated Passives

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Status: 0.3

I. Metal in ICs is not wire in schematic

Metal wires in an integrated circuit comes in two types, copper and aluminium.

Most of the routing layers will be copper. To ensure that the copper ions don't diffuse into the silicon-oxide a barrier material surrounds all copper interconnect.

Copper is too stiff to be wire-bonded. As such, the top layer metals would be aluminium.

Since the routing is so small, we have to care about the parasitic properties of the routing. Below is a table with some common quantities for copper. For example, if we have 1000 μm metal wire with 1 μm width, then it would be approximately 150 Ω, 1 nH , 1 pF and tolerate a maximum of 1 mA DC current.

Parameter	Typ. Value	Unit
Resistance	150	m$\Omega/\square$
Capacitance	1	fF/μm
Inductance	1	nH/mm
Max DC current	1	mA/$\square$

The type of circuit we have determine what we must simulate. Everything needs to be simulated with parasitc capacitance and max current. Only RF, however, usually needs to be simulated with resistance, capacitance, inductance and maximum current.

Circuit type	Must simulate/know
All	C Imax
Analog, Power	R C Imax
Some RF, Some Power	R L C Imax

To simulate the effects of parasitics, we need a description of the technology. A Process Design Kit (PDK). Most PDKs are closely guarded secrets, as they describe many things about the way the foundry makes the integrated circuits.

Some PDKs are open source, however, see Skywater 130 nm and IHP-Open-PDK

In addition to the PDK, we need tools that can calculate from the layout the parasitic elements. Some of the tools are

Layout parasitic extraction tools

- Calibre xRC
- Synopsys StarRC
- Cadence Quantus
- Magic VLSI

3D EM Simulators

- Keysight ADS
- HFSS

Transistor CAD (TCAD)

- Synopsys TCAD

II. Resistors

Sometimes we want a specific resistance. In general, any resistance on IC will vary in absolute value by maybe up to $\pm$ 20 %. The relative size, however, can be controlled to within 0.1 %.

In other words, you can't rely on a 1 kOhm resistor actually being 1 kOhm, it might be 0.8 kOhm. If you have two, however, you can trust that both of them will be 0.8 kOhm.

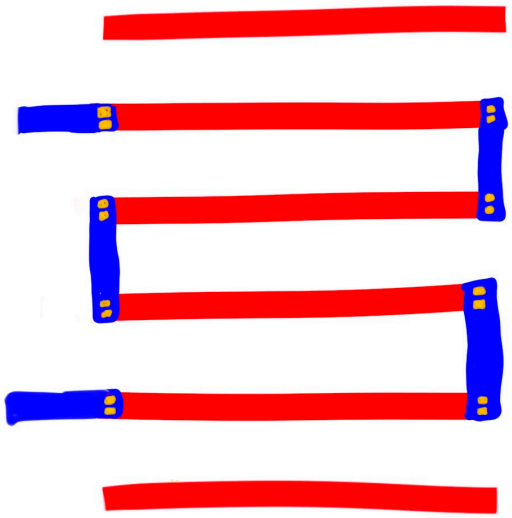
That's why almost all analog circuits rely on the relative sizes of passives, not the absolute value. If a circuit does rely on absolute values, then it usually needs to be trimmed in production.

A. Polysilicon

Can be both N-doped, and P-doped

Often with two flavors, with, and without silicide

Silicide reduces resistance of polysilicon



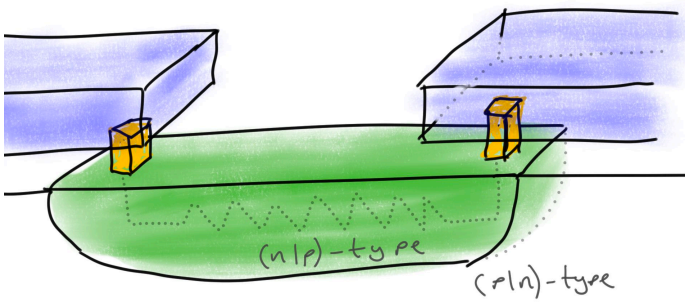
B. Diffusion

Use doped region as resistor

Usually without silicide

Non-linear capacitance

Tricky temperature dependence

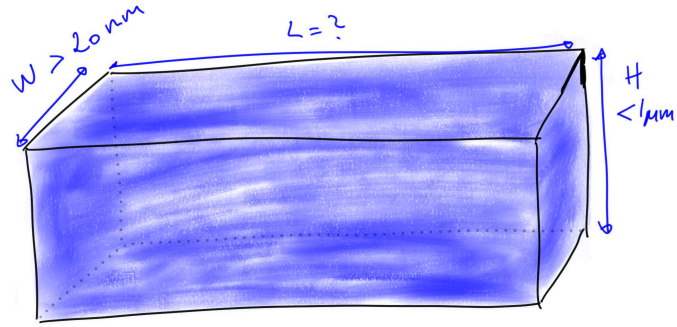


C. Metal

Usually too low omhic to be a useful resistor

Useful for “separating nets” in schematic and layout

Must be considered for power supply and ground routing (high currents)



III. Capacitors

A. What is S, M, L, XL on a chip?

nRF52832

$$3200\mu m \times 3000\mu m = 9600 k\mu m^2$$

S

$$< 5\ k\mu m^2$$

M

$$< 50\ k\mu m^2$$

L

$$< 200\ k\mu m^2$$

XL

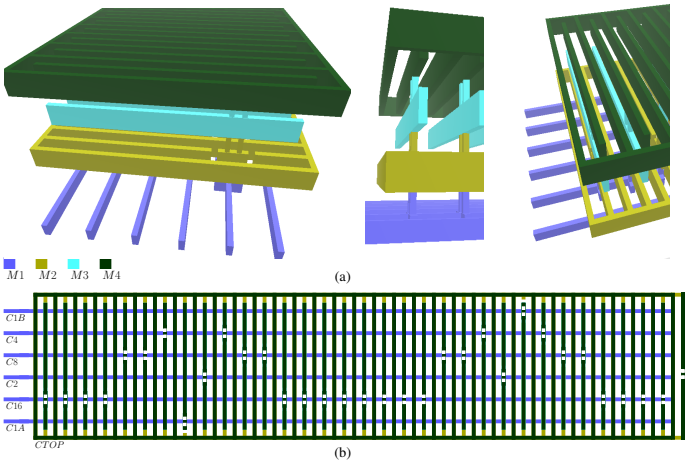
$$> 200\ k\mu m^2$$

B. Metal-Oxide-Metal finger capacitors

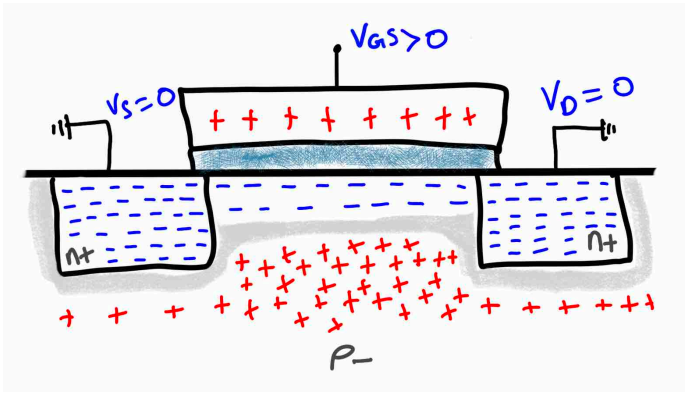
Unit capacitance

$$\approx 1 fF/\mu m^2/layer$$

$$10pF = 100\mu m \times 100\mu m = 10 k\mu m^2$$



C. MOS capacitors




```
dicex/sim/spice/NCHIO/vcap.cir
* gate cap

.include ../../../models/ptm_130.spi

vdrain D 0 dc 1
vgaini G 0 dc 0.5
vbulk B 0 dc 0
vcur S 0 dc 0

M1 D G S B nmos  w=1u  l=1u

.op
```

Moscap is

$$\approx 10 fF/\mu m^2$$

$$10pF = 31\mu m \times 31\mu m \approx 1 k\mu m^2$$

```
dicex/sim/spice/NCHIO/vcap.vlog
Device m1:
    Vgs      (gate-source voltage)          [V] : 0.5
    Vgd      (gate-drain voltage)           [V] : -0.5
    Vds      (drain-source voltage)         [V] : 1
    Vbs      (bulk-source voltage)          [V] : 1.90808e-12
    Vbd      (bulk-drain voltage)           [V] : -1
    Id       (drain current)                [A] : 7.32634e-06
    Is       (source current)               [A] : -7.32633e-06
    Ibd      (bulk-drain current)           [A] : -1.01e-12
    Ibs      (bulk-source current)          [A] : 9.581e-25
    Vt       (threshold voltage)            [V] : 0.378198
    Vgt      (gate overdrive voltage)       [V] : 0.121802
    Vgsteff  (effective vgt)                [V] : 0.12515
    Gm       (transconductance)             [S] : 8.44164e-05
    Gmb      (bulk bias transconductance)   [S] : 2.00071e-05
```

```
Ueff     (mobility)                  [cm^2/Vs] : 417.675
Gds      (channel conductance)             [S] : 1.95043e-07
Rds      (output resistance)             [Ohm] : 5.12708e+06
Vdsat    (drain saturation voltage)        [V] : 0.14171
IC       (inversion coefficient)           [] : 4.42478
Cgs      (gate-source capacitance)         [F] : 9.98457e-15
Csg      (source-gate capacitance)         [F] : 5.86932e-15
Cgd      (gate-drain capacitance)          [F] : 3.98239e-16
Cdg      (drain-gate capacitance)          [F] : 3.91086e-15
Cds      (drain-source capacitance)        [F] : 4.30968e-15
Cgg      (gate-gate capacitance)           [F] : 1.05198e-14
Cdd      (drain-drain capacitance)         [F] : 1.05198e-14
Css      (source-source capacitance)       [F] : 0
Cgb      (gate-bulk capacitance)           [F] : 1.05198e-14
Cbg      (bulk-gate capacitance)           [F] : 1.74123e-15
Cbs      (bulk-source capacitance)         [F] : 8e-16
Cbd      (bulk-drain capacitance)          [F] : 3.97768e-16
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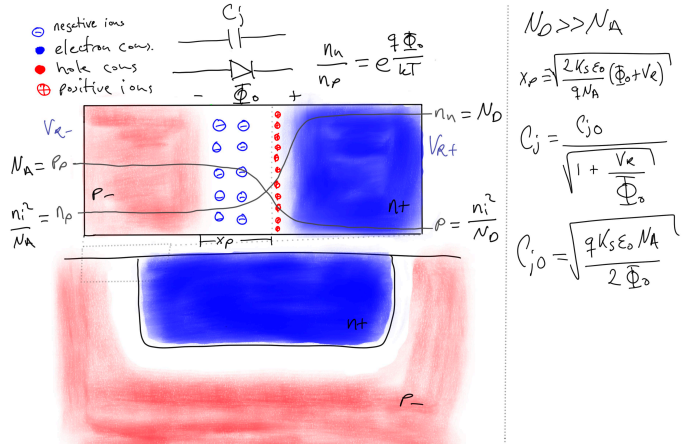
D. Varactors

A varactor is a “variable capacitor”, usually it’s a device that varies the capacitance with the voltage across the device.

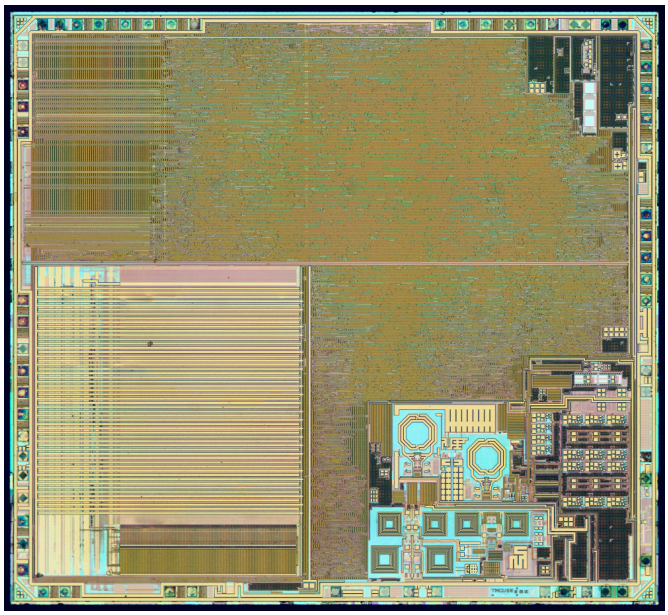


IV. Inductors

Usually two top metals, because they are thick (low ohmic)

Use foundry model

3D electro magnetic simulation often needed



V. Variation in passives

Absolute value for resistors and capacitors

$$\approx \pm 10$$

% to

$$\pm 20$$

%

Relative precision for closely spaced devices

$$\approx$$

0.1 % to 1 %

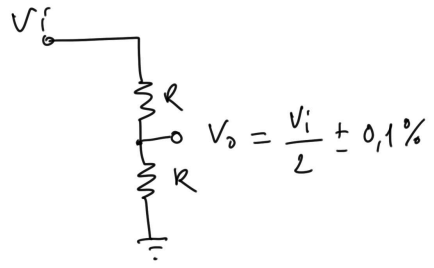
Relative precision for devices on same die

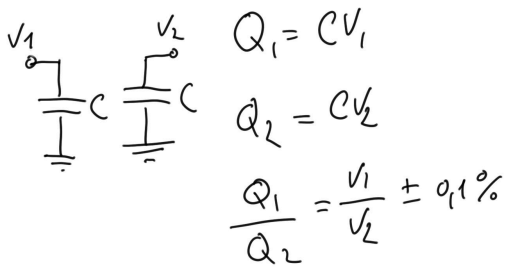
$$> 2$$

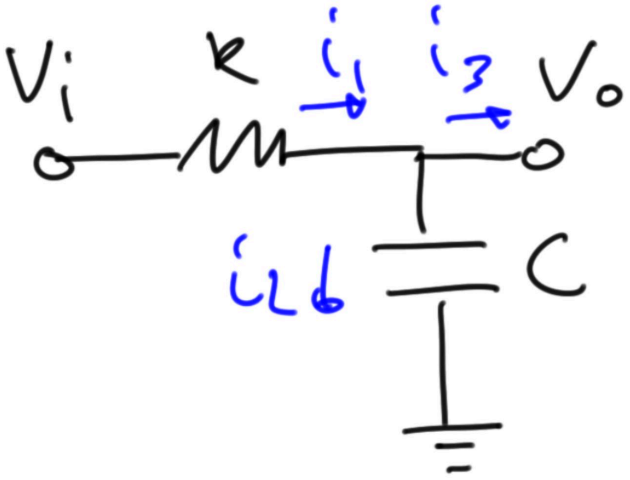
% or more

VI. Relative precision

Resistors and Capacitors can be matched extremely well







$$i_3 = 0 = i_1 - i_2$$
$$0 = \frac{V_i - V_o}{R} - \frac{V_o}{1/sC}$$

$$0 = V_i - V_o - V_o sRC$$
$$V_o(1 + sRC) = V_i$$

$$\frac{V_o}{V_i} = \frac{1}{1 + sRC}$$

Assume standard deviation (σ)[1] of $\sigma_R = 20$ %, $\sigma_C = 20$ %

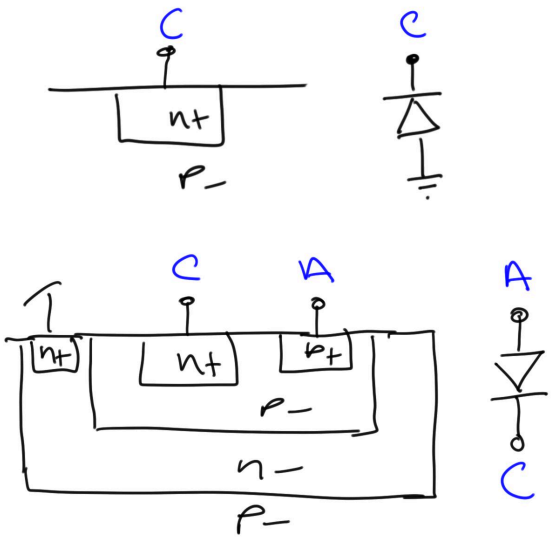
$$\sigma_{RC} = \sqrt{0.2^2 + 0.2^2} = 28$$

%

VII. Diodes

Many, many ways

Reverse bias diodes to ground are useful for signals with long routing to transistor gate. Protects gate from breakdown during chemical mechanical polish.



[1] If you don't remember how standard deviation works, read Introduction to mathematics of noise sources

Carsten Wulff received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electronics and Telecommunication, Norwegian University of Science and Technology (NTNU), in 2002 and 2008, respectively. During his Ph.D. work at NTNU, he worked on open-loop sigma-delta modulators and analog-to-digital converters in nanoscale CMOS technologies. In 2006-2007, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. Since 2008 he's been with Nordic Semiconductor in various roles, from analog designer, to Wireless Group Manager, to currently Principle IC Scientist. From 2014-2017 he did a part time Post.Doc focusing on compiled, ultra low power, SAR ADCs in nanoscale technologies. He's also an Adjunct Associate Professor at NTNU. His present research interests includes analog and mixed-signal CMOS design, design of high-efficiency analog-to-digital converters and low-power wireless transceivers. He is the developer of Custom IC Compiler, a general purpose integrated circuit compiler, and makes the occational video on analog integrated circuits at https://www.youtube.com/@analogicus. For full CV see https://analogicus.com/markdown-cv/.