

Circuits

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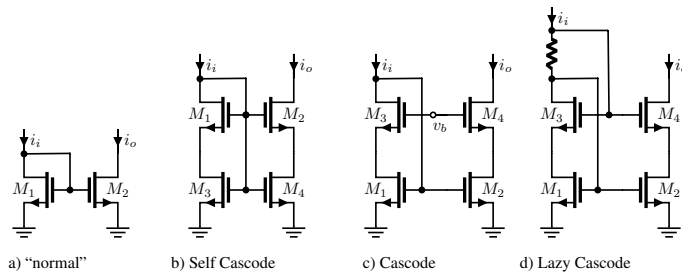
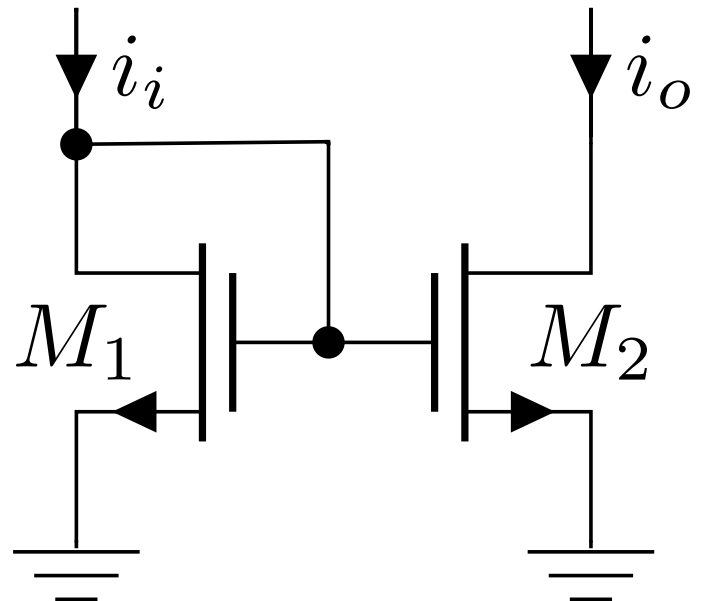
I. CURRENT MIRRORS

MOSFETs need a current for the transistor to be biased in the correct operating region. The current must come from somewhere, we'll look at bias generators later. Usually there is a central bias circuit that provides a single, good, reference current.

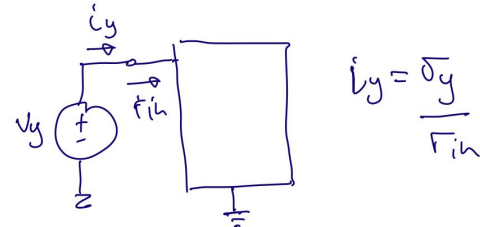
On an IC, however, there will be many circuits, and they all need a bias current (usually). As such, we need a circuit to copy a current.

In the figure below you can see a selection of current mirrors. They all do the same thing. Try to ensure that i_i and i_o are the same current.

Which one we choose is usually determined by what we mean by $i_i = i_o$. Do we mean "within $\pm 10\%$ ", or "within $\pm 2\%$ ".



1) *Input resistance:* To see the small signal input resistance we can apply a test voltage to the diode connected resistor, as shown in the figure below.



A. Normal current mirror

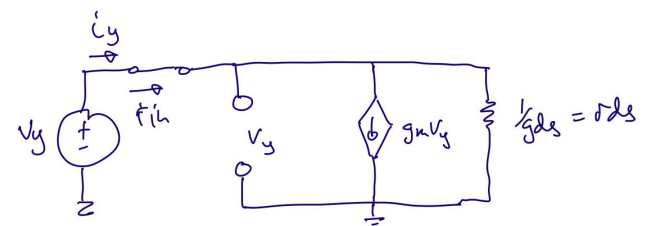
The normal current mirror consists of a diode connected transistor (M_1) and a common source transistor M_2 .

If we assume infinite output resistance of the MOSFETs, then the drain voltage does not affect the current.

If the two transistors are the same size, threshold voltage, mobility, etc, and they have the same gate-source voltage, then the current in them must be the same.

A current pushed into M_1 will cause the V_{GS1} to rise, and at some point, find a stable point where the current pushed in is equal to the current in M_1

M_2 will see the same $V_{GS1} = V_{GS2}$ so the current will be the same, provided the voltage at i_o is sufficient to pinch-off the channel of M_2 , or the $V_{DS2} \approx 3kT/q$ if the transistor is in weak-inversion.



Observe the current

$$i_y = g_{ds}v_y + g_mv_y$$

While the input resistance

$$r_{in} = \frac{v_y}{i_y} = \frac{1}{g_m + g_{ds}}$$

which, assuming $g_{ds} \gg g_m$, reduces to

$$r_{in} \approx \frac{1}{g_m}$$

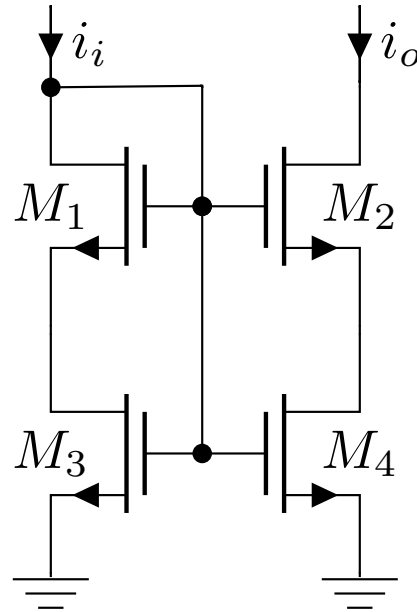
Assume now I apply $1 \mu A$ current to the diode connected transistor, and the $g_m = 1 \mu S$.

Would the voltage be $v_y = r_{in} i_y = \frac{1 \mu A}{1 \mu S} = 1 V$? NO! It's important to understand the difference between the small signal input resistance, and the large signal impedance.

The large signal impedance is a highly non-linear function (we've seen before that the current in a MOSFET has both an exponential, and a square-law, and sometimes a linear with voltage), as such, there is no single function describing what the gate-source voltage will be.

To see the DC voltage, apply a current in SPICE, and use a simulator to find the voltage.

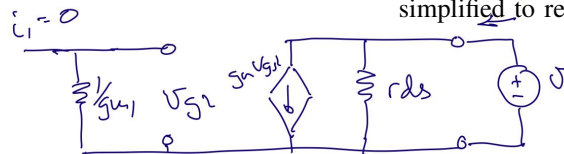
B. Source degeneration



What is the operating region of M3 and M4?

What is the operating region of M1 and M2?

1) Input resistance: M1 and M2 are in linear region, can be simplified to resistors

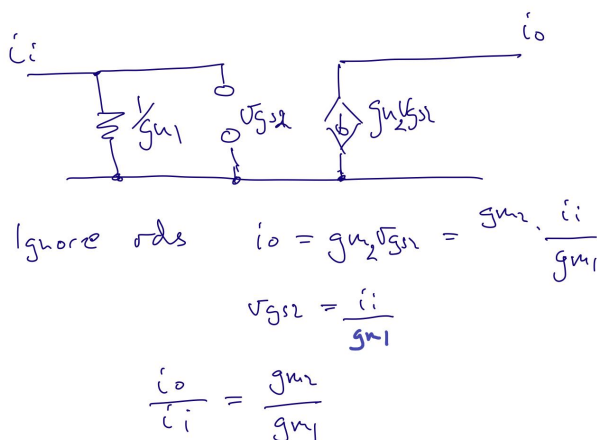


$$r_{in} = \frac{1}{g_{m1}} + R_s$$

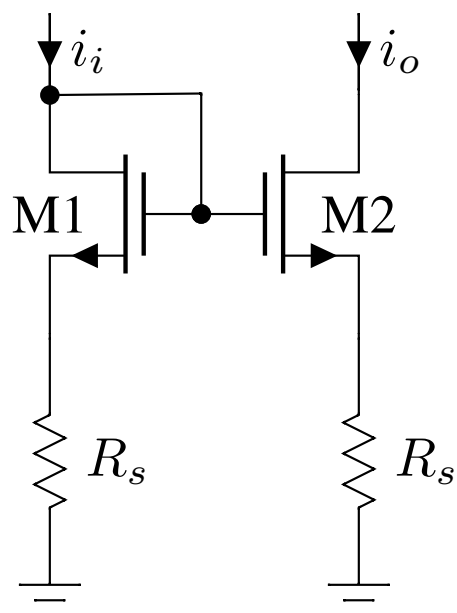
v_y does not affect v_{gs2}

$$r_{out} = r_{ds}$$

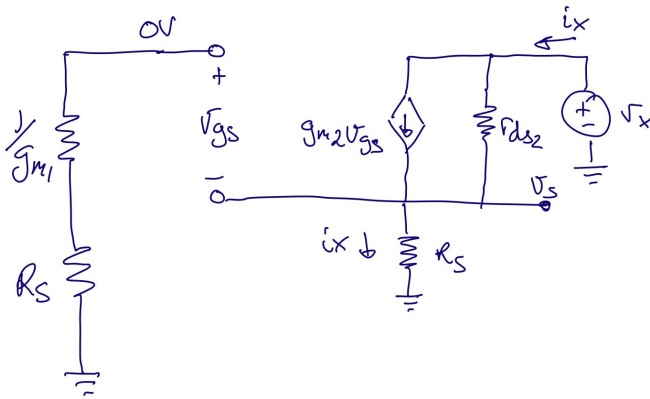
2) Output resistance:



3) Current gain:



C. Output resistance



$$v_{gs} = -v_s$$

$$v_s = i_x R_s$$

$$r_{out} = \frac{v_x}{i_x}$$

$$i_x = g_{m2} v_{gs} + \frac{v_x - v_s}{r_{ds2}}$$

$$i_x = -i_x g_{m2} R_s + \frac{v_x - i_x R_s}{r_{ds2}}$$

$$v_x = i_x [r_{ds2} + R_s (g_{m2} r_{ds2} + 1)]$$

Rearranging

$$r_{out} = r_{ds2} [1 + R_s (g_{m1} + g_{ds2})] \approx r_{ds2} [1 + g_{m1} R_s]$$

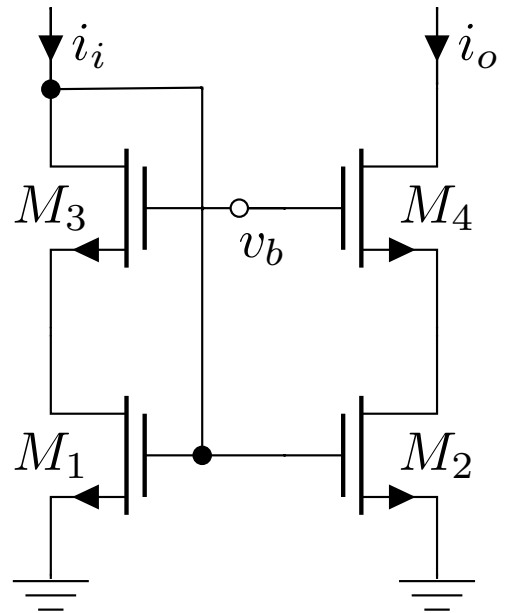
1) Cascode output resistance: From source degeneration (ignoring bulk effect)

$$r_{out} = r_{ds4} [1 + R_s (g_{m4} + g_{ds4})]$$

$$R_s = r_{ds2}$$

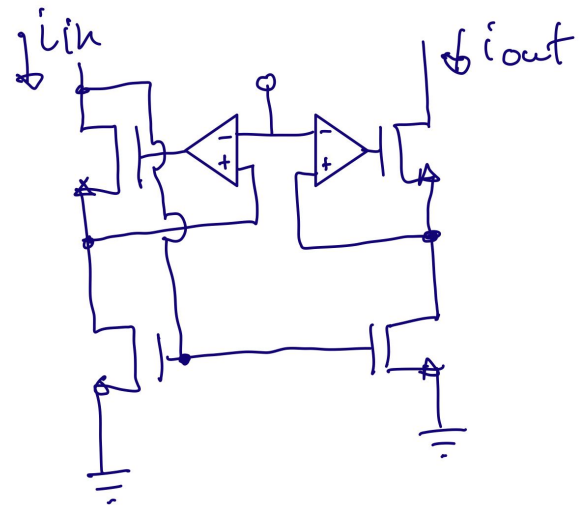
$$r_{out} = r_{ds4} [1 + r_{ds2} (g_{m4} + g_{ds4})]$$

$$r_{out} \approx r_{ds2} (r_{ds4} g_{m4})$$



2) Active cascodes:

$$r_{out} \approx r_{ds2} (A r_{ds4} g_{m4})$$



II. AMPLIFIERS

III. SOURCE FOLLOWER

Input resistance

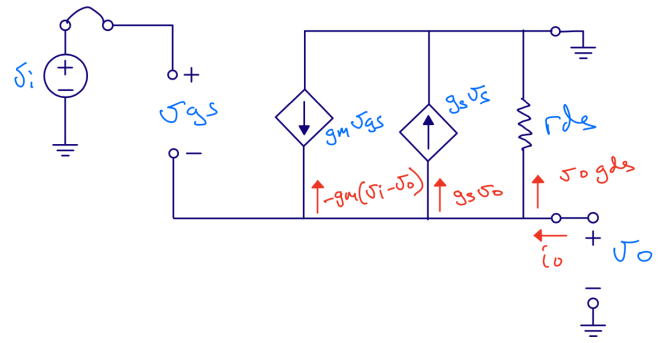
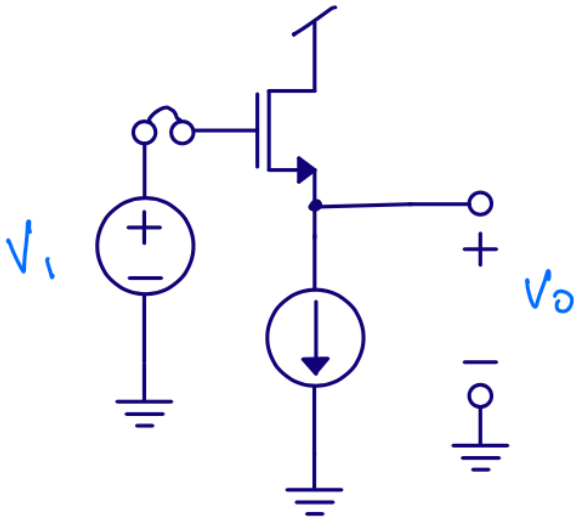
$$\approx \infty$$

Gain

$$A = \frac{v_o}{v_i}$$

Output resistance

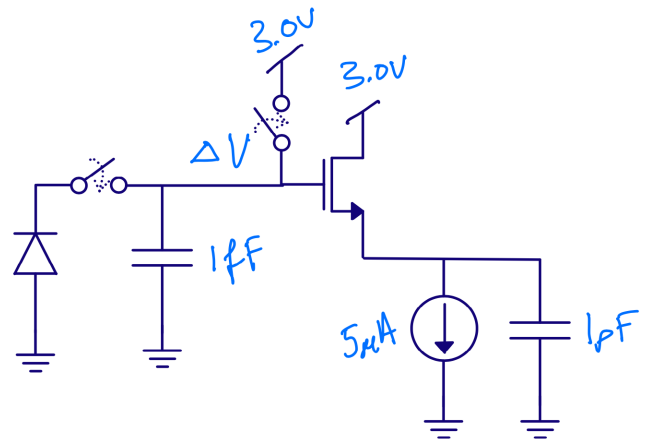
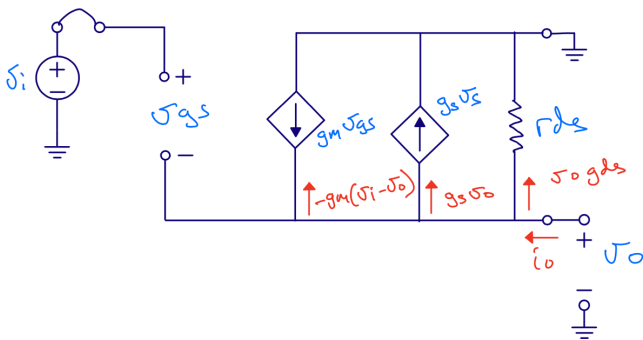
$$r_{out}$$



B. Why use a source follower?

Assume 100 electrons

$$\Delta V = Q/C = -1.6 \times 10^{-19} \times 100 / (1 \times 10^{-15}) = -16 \text{ mV}$$



A. Output resistance

$$i_o = v_o(g_{ds} + g_s) - g_m v_i + v_o g_m$$

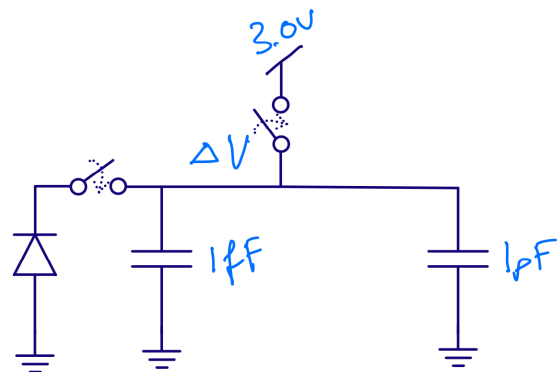
$$v_i = 0$$

$$i_o = v_o(g_{ds} + g_s + g_m)$$

$$r_{out} = \frac{v_o}{i_o} = \frac{1}{g_m + g_{ds} + g_s}$$

$$r_{out} \approx \frac{1}{g_m}$$

$$\Delta V = Q/C = -1.6 \times 10^{-19} \times 100 / (1 \times 10^{-12}) = -16 \text{ uV}$$

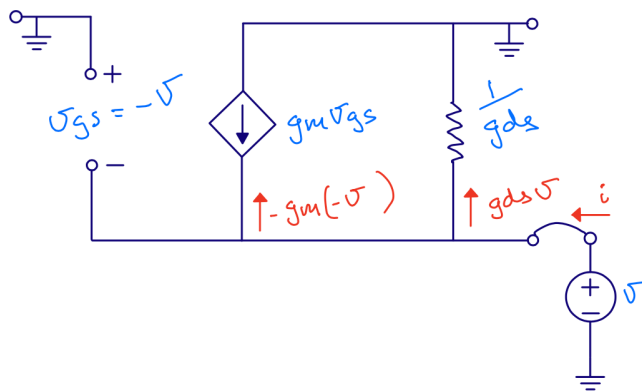
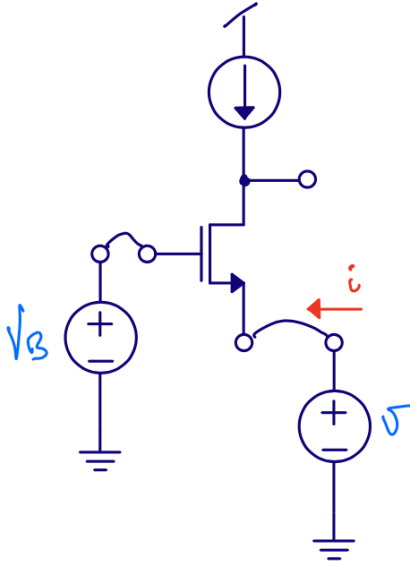


IV. COMMON GATE

Input resistance

Gain

Output resistance



A. Input resistance

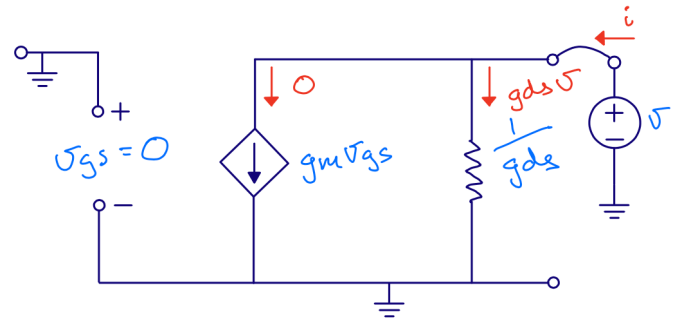
$$i = g_m v + g_{ds} v$$

$$r_{in} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m}$$

However, we've ignored load resistance.

$$r_{in} \approx \frac{1}{g_m} \left(1 + \frac{R_L}{r_{ds}} \right)$$

B. Output resistance



C. Gain

$$i_o = -g_m v_i + \frac{v_o - v_i}{r_{ds}}$$

$$i_o = 0$$

$$0 = -g_m v_i r_{ds} + v_o - v_i$$

$$v_i (1 + g_m r_{ds}) = v_o$$

$$\frac{v_o}{v_i} = 1 + g_m r_{ds}$$

We've ignored bulk effect (

$$g_s$$

), source resistance (

$$R_S$$

) and load resistance (

$$R_L$$

)

$$A = \frac{(g_m + g_s + g_{ds})(R_L || r_{ds})}{1 + R_S \left(\frac{g_m + g_s + g_{ds}}{1 + R_L / r_{ds}} \right)}$$

If

$$R_L \gg r_{ds}$$

,

$$R_S = 0$$

and

$$g_s = 0$$

$$A = \frac{(g_m + g_{ds})r_{ds}}{1} = 1 + g_m r_{ds}$$

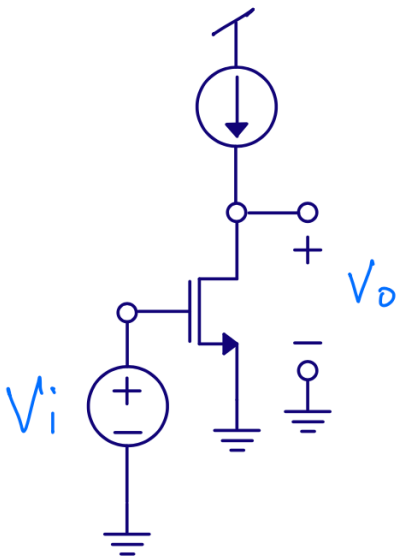
V. COMMON SOURCE

$$r_{in} \approx \infty$$

$$r_{out} = r_{ds}$$

, it's same circuit as the output of a current mirror

Gain



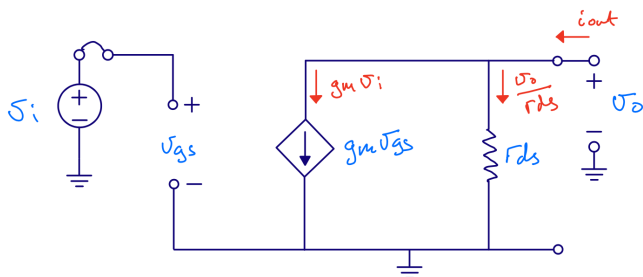
A. Gain

$$i_o = g_m v_i + \frac{v_o}{r_{ds}}$$

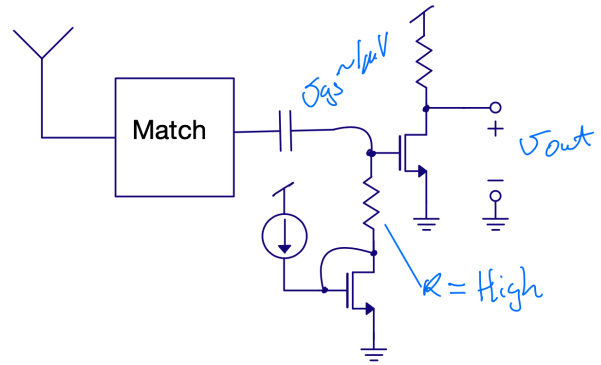
$$i_o = 0$$

$$-g_m v_i = \frac{v_o}{r_{ds}}$$

$$\frac{v_o}{v_i} = -g_m r_{ds}$$



B. Why common source?



VI. DIFFERENTIAL PAIR

Input resistance

$$r_{in} \approx \infty$$

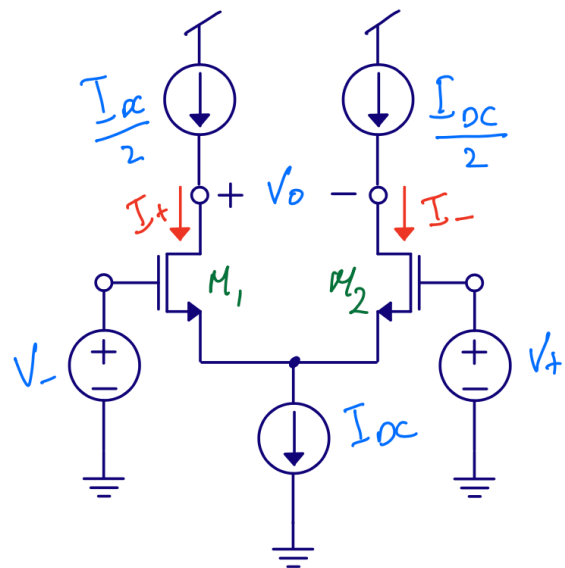
Gain

$$A = g_m r_{ds}$$

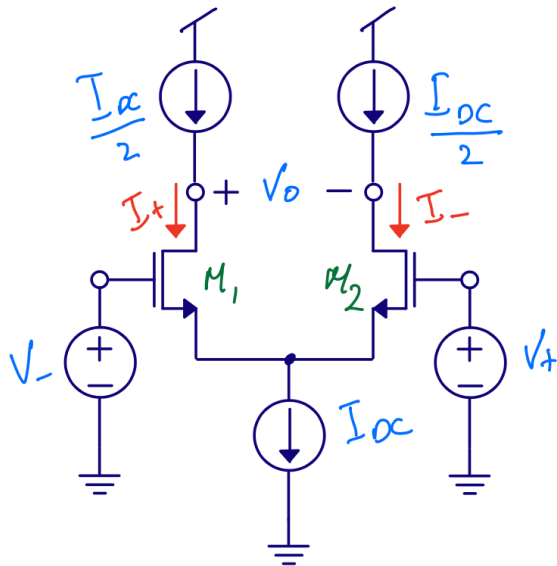
Output resistance

$$r_{out} = r_{ds}$$

Best analyzed with T model of transistor (see CJM page 31)



A. Diff pairs are cool



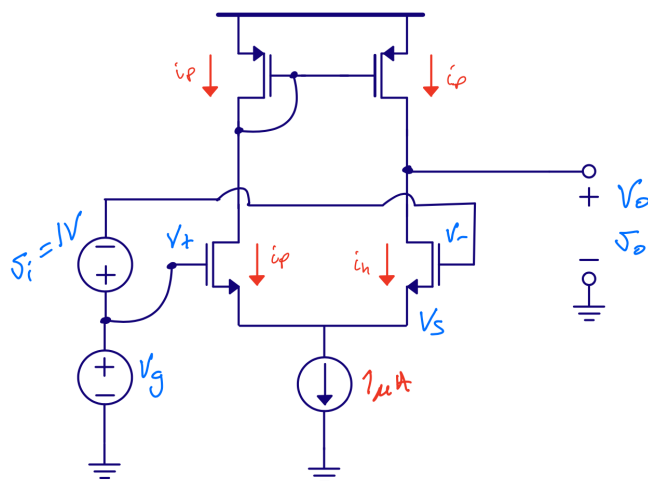
Can choose between

$$v_o = g_m r_{ds} v_i$$

and

$$v_o = -g_m r_{ds} v_i$$

by flipping input (or output) connections



he worked on open-loop sigma-delta modulators and analog-to-digital converters in nanoscale CMOS technologies. In 2006-2007, he was a Visiting Researcher with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. Since 2008 he's been with Nordic Semiconductor in various roles, from analog designer, to Wireless Group Manager, to currently Principle IC Scientist. From 2014-2017 he did a part time Post.Doc focusing on compiled, ultra low power, SAR ADCs in nanoscale technologies. He's also an Adjunct Associate Professor at NTNU. His present research interests includes analog and mixed-signal CMOS design, design of high-efficiency analog-to-digital converters and low-power wireless transceivers. He is the developer of Custom IC Compiler, a general purpose integrated circuit compiler, and makes the occasional video on analog integrated circuits at <https://www.youtube.com/@analogicus>. For full CV see <https://analogicus.com/markdown-cv/>.



Carsten Wulff received the M.Sc. and Ph.D. degrees in electrical engineering from the Department of Electronics and Telecommunication, Norwegian University of Science and Technology (NTNU), in 2002 and 2008, respectively. During his Ph.D. work at NTNU,